UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, DC 20549

FORM 8-K

CURRENT REPORT
Pursuant to Section 13 or 15(d)
of the Securities Exchange Act of 1934

Date of Report (Date of earliest event reported) November 11, 2025

QuickLogic Corporation

(Exact name of registrant as specified in its charter)

Delaware	**000-22671**	**77-0188504**
(State or other jurisdiction of incorporation)	**(Commission File Number)**	**(IRS Employer Identification No.)**
2220 Lundy Avenue, San Jose, CA (Address of principal executive offices)		**95131-1816 (Zip Code)**

Registrant's telephone number, including area code (408) 990-4000

N/A
(Former name or former address, if changed since last report)

Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions (see General Instruction A.2. below):

☐ Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425)

☐ Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12)

☐ Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b))

☐ Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4(c))

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	Trading Symbol(s)	Name of each exchange on which registered
Common Stock, par value $.001 per share	QUIK	The Nasdaq Capital Market

Indicate by check mark whether the registrant is an emerging growth company as defined in Rule 405 of the Securities Act of 1933 (§230.405 of this chapter) or Rule 12b-2 of the Securities Exchange Act of 1934 (§240.12b-2 of this chapter).

Emerging growth company ☐

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act. ☐

Item 2.02 Results of Operation and Financial Condition.

On November 11, 2025, QuickLogic Corporation (“QuickLogic”) issued a press release and held a conference call announcing its financial results for the fiscal third quarter ended September 28, 2025. A copy of the press release and a full transcript of the conference call (the "Transcript") are attached hereto as Exhibit 99.1 and Exhibit 99.2, respectively, and are incorporated herein by reference.

QuickLogic is making reference to non-GAAP financial information in the press release. The Transcript also contains certain non-GAAP financial measures. A reconciliation of GAAP to non-GAAP results is provided in the attached Exhibit 99.1 press release.

Item 7.01 Regulation FD Disclosure.

On November 11, 2025, QuickLogic Corporation (“QuickLogic”) issued a press release regarding its financial results for the fiscal third quarter ended September 28, 2025. A copy of the press release is attached hereto as Exhibit 99.1 and is incorporated herein by reference.

The information in this Current Report, including Exhibits 99.1 and 99.2, is furnished and shall not be deemed “filed” for purposes of Section 18 of the Exchange Act, or otherwise subject to liabilities under that section, and shall not be deemed to be incorporated by reference into the filings of the registrant under the Securities Act of 1933, as amended, or the Exchange Act, regardless of any general incorporation language in such filings. In addition, the press release and Transcript furnished as exhibits to this report includes "safe harbor" language pursuant to the Private Securities Litigation Reform Act of 1995, stating that certain statements about QuickLogic's business contained in the press release and Transcript are "forward-looking" rather than historic.

Disclaimer: The information contained in the Transcript furnished as Exhibit 99.2 is a textual representation of an audio recording of the earnings call and while efforts are made to provide an accurate transcription, there may be material errors, omissions, or inaccuracies in the reporting of the substance of the audio recording. The Company does not assume responsibility for any investment or other decisions made based upon the information provided in this Transcript. Users are advised to review the audio recording and the Company's SEC filings before making any investment or other decisions. An archived recording of the earnings call will be available for 30 days on the Company's Investor Relations section of the Company's website at https://ir.quicklogic.com/ir-calendar.

Item 9.01 Financial Statement and Exhibits.

(d) Exhibits

99.1	Press release of QuickLogic Corporation reporting financial results for the fiscal third quarter ended September 28, 2025.
99.2	Transcript of QuickLogic Corporation conference call announcing financial results for the fiscal third quarter ended September 28, 2025
104	Cover Page Interactive Data File (embedded within the Inline XBRL document)

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, as amended, the registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

Date: November 12, 2025

QuickLogic Corporation

/s/ Elias Nader
Elias Nader
Chief Financial Officer, and Senior Vice-President, Finance

QuickLogic Reports Fiscal Third Quarter 2025 Financial Results

SAN JOSE, Calif. – November 11, 2025 - QuickLogic Corporation (NASDAQ: QUIK) ("QuickLogic" or the "Company"), a developer of embedded FPGA (eFPGA) IP, ruggedized FPGAs, and Endpoint AI solutions, today announced its financial results for the fiscal third quarter that ended September 28, 2025.

Recent Highlights

- Won a $1 million eFPGA Hard IP contract for a high-performance data-center ASIC, which continues to expand our success in commercial markets
- Expanded our involvement with Defense Industrial Base entity specializing in cyber-security for strategic and tactical weapons systems
- A significant rebound of USG Strategic Radiation Hardened FPGA Program expected to contribute to fourth-quarter revenue growth
- Appointed Ron Shelton, CFO of Syntiant Corp., to the Board of Directors and Chair of the Audit Committee

"We have logged significant progress during the last three months," said Brian Faith, CEO of QuickLogic. "Our investment to accelerate the fabrication of our Strategic Rad Hard FPGA Test Chip is being very well received by potential customers. As a matter of fact, we anticipate receiving orders for our upcoming SRH FPGA Dev Kit, as well as several new eFPGA Hard IP contracts, during the coming weeks."

Fiscal Third Quarter 2025 Financial Results

Total revenue from continuing operations for the third quarter of fiscal 2025 was $2.0 million, a decrease of 51.8% compared with the third quarter of 2024 and a decrease of 45.0% compared with the second quarter of 2025.

New product revenue from continuing operations was approximately $1.0 million in the third quarter of 2025, a decrease of $2.5 million, or 72.6%, compared with the third quarter of 2024 and a decrease of $1.9 million, or 67.3%, compared with the second quarter of 2025.

Mature product revenue from continuing operations was $1.1 million in the third quarter of 2025. This compares to $0.7 million in the third quarter of 2024 and $0.8 million in the second quarter of 2025.

Third quarter 2025 GAAP gross margin from continuing operations was (23.3%) compared with 59.1% in the third quarter of 2024 and 25.9% in the second quarter of 2025.

Third quarter 2025 non-GAAP gross margin from continuing operations was (11.9%) compared with 64.7% in the third quarter of 2024 and 31.0% in the second quarter of 2025.

Third quarter 2025 GAAP operating expenses from continuing operations were $3.5 million compared with $4.1 million in the third quarter of 2024 and $3.5 million in the second quarter of 2025.

Third quarter 2025 non-GAAP operating expenses from continuing operations were $2.9 million compared with $3.0 million in the third quarter of 2024 and $2.5 million in the second quarter of 2025.

Third quarter 2025 GAAP net loss was ($4.0 million), or ($0.24) per share, compared with a net loss of ($2.1 million), or ($0.14) per share, in the third quarter of 2024, and a net loss of ($2.7 million), or ($0.17) per share, in the second quarter of 2025.

Third quarter 2025 non-GAAP net loss was ($3.2 million), or ($0.19) per share, compared with a net loss of ($0.9 million), or ($0.07) per share, in the third quarter of 2024, and a net loss of ($1.5 million), or ($0.09) per share, in the second quarter of 2025.

Conference Call

QuickLogic will hold a conference call at 2:30 p.m. Pacific Time / 5:30 p.m. Eastern Time today, November 11, 2025, to discuss its current financial results. The conference call will be webcast on QuickLogic's IR Site Events Page at https://ir.quicklogic.com/ir-calendar. To join the live conference, you may dial (877) 407-0792 and international participants should dial (201) 689-8263 by 2:20 p.m. Pacific Time. No Passcode is needed to join the conference call. A recording of the call will be available approximately one hour after completion. To access the recording, please call (844) 512-2921 and reference the passcode 13756624.

The call recording, which can be accessed by phone, will be archived through November 18, 2025, and the webcast will be available for 12 months on the Company's website.

About QuickLogic

QuickLogic is a fabless semiconductor company specializing in embedded FPGA (eFPGA) Hard IP, discrete FPGAs, and endpoint AI solutions. QuickLogic's unique approach combines cutting-edge technology with open-source tools to deliver highly customizable low-power solutions for aerospace and defense, industrial, computing, and consumer markets. For more information, visit www.quicklogic.com.

QuickLogic uses its website (www.quicklogic.com), the company blog (https://www.quicklogic.com/blog/), corporate X account (@QuickLogic_Corp), Facebook page (https://www.facebook.com/QuickLogic), and LinkedIn page (https://www.linkedin.com/company/13512/) as channels of distribution of information about its products, its planned financial and other announcements, its attendance at upcoming investor and industry conferences, and other matters. Such information may be deemed material information, and QuickLogic may use these channels to comply with its disclosure obligations under Regulation FD. Therefore, investors should monitor the Company's website and its social media accounts in addition to following the Company's press releases, SEC filings, public conference calls, and webcasts.

Non-GAAP Financial Measures

QuickLogic reports financial information in accordance with United States Generally Accepted Accounting Principles, or U.S. GAAP, but believes that non-GAAP financial measures are helpful in evaluating its operating results and comparing its performance to comparable companies. Accordingly, the Company excludes certain charges related to stock-based compensation and restructuring costs, in calculating non-GAAP (i) income (loss) from operations, (ii) net income (loss), (iii) net income (loss) per share, and (iv) gross margin percentage. The Company provides this non-GAAP information to enable investors to evaluate its operating results in a manner like how the Company analyzes its operating results and to provide consistency and comparability with similar companies in the Company's industry.

Management uses the non-GAAP measures, which exclude gains, losses, and other charges that are considered by management to be outside of the Company's core operating results, internally to evaluate its operating performance against results in prior periods and its operating plans and forecasts. In addition, the non-GAAP measures are used to plan for the Company's future periods and serve as a basis for the allocation of the Company's resources, management of operations and the measurement of profit-dependent cash, and equity compensation paid to employees and executive officers.

Investors should note, however, that the non-GAAP financial measures used by QuickLogic may not be the same non-GAAP financial measures and may not be calculated in the same manner as that of other companies. QuickLogic does not itself, nor does it suggest that investors should, consider such non-GAAP financial measures alone or as a substitute for financial information prepared in accordance with U.S. GAAP. A reconciliation of U.S. GAAP financial measures to non-GAAP financial measures is included in the financial statements portion of this press release. Investors are encouraged to review the related U.S. GAAP financial measures and the reconciliation of non-GAAP financial measures with their most directly comparable U.S. GAAP financial measures.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. These forward-looking statements include, without limitation, statements regarding our future profitability and cash flows, expectations regarding our future business and statements regarding the timing, milestones, and payments related to our government contracts, statements regarding the use of the Company's ATM program, and statements regarding our ability to successfully exit SensiML, and actual results may differ due to a variety of factors including: delays in the market acceptance of the Company's new products; the ability to convert design opportunities into customer revenue; our ability to replace revenue from end-of-life products; the level and timing of customer design activity; the market acceptance of our customers' products; the risk that new orders may not result in future revenue; our ability to introduce and produce new products based on advanced wafer technology on a timely basis; our ability to adequately market the low power, competitive pricing and short time-to-market of our new products; intense competition by competitors; our ability to hire and retain qualified personnel; changes in product demand or supply; general economic conditions; political events, international trade disputes, natural disasters and other business interruptions that could disrupt supply or delivery of, or demand for, the Company's products; and changes in tax rates and exposure to additional tax liabilities. These and other potential factors and uncertainties that could cause actual results to differ materially from the results contemplated or implied are described in more detail in the Company's public reports filed with the U.S. Securities and Exchange Commission (the "SEC"), including the risks discussed in the "Risk Factors" section in the Company's Annual Reports on Form 10-K, Quarterly Reports on Form 10-Q and in the Company's prior press releases, which are available on the Company's Investor Relations website at http://ir.quicklogic.com/, and on the SEC website at www.sec.gov/. In addition, please note that the date of this press release is November 11, 2025, and any forward-looking statements contained herein are based on management's current expectations and assumptions that we believe to be reasonable as of this date. We are not obliged to update these statements due to latest information or future events.

Company Contact

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IR Contact

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CODE: QUIK-E

–Tables Follow –

QUICKLOGIC CORPORATION
CONDENSED CONSOLIDATED STATEMENTS OF OPERATIONS
(in thousands, except per share amounts)
(Unaudited)

	Three Months Ended			Nine Months Ended	
	September 28, 2025	September 29, 2024	June 29, 2025	September 28, 2025	September 29, 2024
Revenue	$ 2,029	$ 4,209	$ 3,687	$ 10,041	$ 13,974
Cost of revenue	2,501	1,721	2,733	7,682	5,440
Gross profit (loss)	(472)	2,488	954	2,359	8,534
Operating expenses:					
Research and development	1,398	1,798	1,193	3,859	4,466
Selling, general and administrative	2,057	2,292	1,962	6,555	6,738
Impairment charges	—	—	300	300	—
Restructuring costs	—	—	21	75	—
Total operating expense	3,455	4,090	3,476	10,789	11,204
Operating income (loss)	(3,927)	(1,602)	(2,522)	(8,430)	(2,670)
Interest expense	(87)	(187)	(108)	(292)	(295)
Interest and other (expense) income, net	9	(26)	(30)	(28)	(5)
Income (loss) before income taxes	(4,005)	(1,815)	(2,660)	(8,750)	(2,970)
(Benefit from) provision for income taxes	(1)	13	1	5	14
Net income (loss) from continuing operations	(4,004)	(1,828)	(2,661)	(8,755)	(2,984)
Net income (loss) from discontinued operations, net of taxes and inclusive of $87 in restructuring costs for the nine months ended September 28, 2025	(3)	(266)	(9)	(113)	(552)
Net income (loss)	$ (4,007)	$ (2,094)	$ (2,670)	$ (8,868)	$ (3,536)
Net income (loss) from continuing operations per share:					
Basic	$ (0.24)	$ (0.13)	$ (0.17)	$ (0.55)	$ (0.21)
Diluted	$ (0.24)	$ (0.13)	$ (0.17)	$ (0.55)	$ (0.21)
Net income (loss) per share:					
Basic	$ (0.24)	$ (0.14)	$ (0.17)	$ (0.56)	$ (0.25)
Diluted	$ (0.24)	$ (0.14)	$ (0.17)	$ (0.56)	$ (0.25)
Weighted average shares outstanding:					
Basic	16,516	14,555	15,884	15,957	14,390
Diluted	16,516	14,555	15,884	15,957	14,390

Note: Net income (loss) equals total comprehensive income (loss) for all periods presented. Additionally, the Company notes that income taxes related to discontinued operations were immaterial in nature for the periods presented and as such, only net income (loss) from discontinued operations was reported herein.

QUICKLOGIC CORPORATION
CONDENSED CONSOLIDATED BALANCE SHEETS
(in thousands)
(Unaudited)

	September 28, 2025	December 29, 2024
ASSETS		
Current assets:		
Cash, cash equivalents and restricted cash	$ 17,343	$ 21,859
Accounts receivable, net of allowance for credit losses of $0 as of September 28, 2025 and December 29, 2024	2,034	2,426
Contract assets	1,396	2,682
Note receivable, current	1,388	—
Inventories	869	940
Prepaid expenses and other current assets	1,261	1,666
Assets of business held for sale, net	10	31
Total current assets	24,301	29,604
Property and equipment, net	16,647	15,699
Capitalized internal-use software, net	1,081	711
Right of use assets, net	540	758
Intangible assets, net	349	378
Non-marketable equity investment	—	300
Inventories, non-current	618	718
Note receivable, non-current	—	1,292
Other assets	227	117
Assets of business held for sale, net	2,355	2,356
TOTAL ASSETS	$ **46,118**	$ **51,933**
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Revolving line of credit	$ 15,000	$ 18,000
Trade payables	2,763	3,097
Accrued liabilities	952	1,587
Deferred revenue	382	444
Notes payable, current	1,234	1,928
Lease liabilities, current	311	284
Liabilities of business held for sale	(1)	57
Total current liabilities	20,641	25,397
Long-term liabilities:		
Lease liabilities, non-current	218	447
Notes payable, non-current	529	1,202
Total liabilities	21,388	27,046
Commitments and contingencies		
Stockholders' equity:		
Preferred stock, $0.001 par value; 10,000 shares authorized; no shares issued and outstanding	—	—
Common stock, $0.001 par value; 200,000 authorized; 16,768 and 15,336 shares issued and outstanding as of September 28, 2025 and December 29, 2024, respectively	17	15
Additional paid-in capital	342,977	334,268
Accumulated deficit	(318,264)	(309,396)
Total stockholders' equity	24,730	24,887
TOTAL LIABILITIES AND STOCKHOLDERS' EQUITY	$ **46,118**	$ **51,933**

QUICKLOGIC CORPORATION
SUPPLEMENTAL RECONCILIATIONS OF US GAAP AND NON-GAAP FINANCIAL MEASURES
(in thousands, except per share amounts and percentages)
(Unaudited)

	Three Months Ended			Nine Months Ended	
	September 28, 2025	September 29, 2024	June 29, 2025	September 28, 2025	September 29, 2024
US GAAP operating income (loss)	$ **(3,927)**	$ **(1,602)**	$ **(2,522)**	$ **(8,430)**	$ **(2,670)**
Adjustment for stock-based compensation within:					
Cost of revenue	231	237	189	578	675
Research and development	96	428	205	443	729
Selling, general and administrative	501	645	449	1,586	2,131
Adjustment for impairment charges	—	—	300	300	—
Adjustment for restructuring costs	—	—	21	75	—
Non-GAAP operating income (loss)	$ **(3,099)**	$ **(292)**	$ **(1,358)**	$ **(5,448)**	$ **865**
US GAAP net income (loss) from continuing operations	$ **(4,004)**	$ **(1,828)**	$ **(2,661)**	$ **(8,755)**	$ **(2,984)**
Adjustment for stock-based compensation within:					
Cost of revenue	231	237	189	578	675
Research and development	96	428	205	443	729
Selling, general and administrative	501	645	449	1,586	2,131
Adjustment for impairment charges	—	—	300	300	—
Adjustment for restructuring costs	—	—	21	75	—
Non-GAAP net income (loss) from continuing operations	$ **(3,176)**	$ **(518)**	$ **(1,497)**	$ **(5,773)**	$ **551**
US GAAP net income (loss) from discontinued operations	$ **(3)**	$ **(266)**	$ **(9)**	$ **(113)**	$ **(552)**
Adjustment for stock-based compensation within:					
Research and development	—	(105)	—	(32)	147
Adjustment for restructuring costs	—	—	—	87	—
Non-GAAP net income (loss) from discontinued operations	$ **(3)**	$ **(371)**	$ **(9)**	$ **(58)**	$ **(405)**
Non-GAAP net income (loss)	$ **(3,179)**	$ **(889)**	$ **(1,506)**	$ **(5,831)**	$ **146**
US GAAP net income (loss) from continuing operations per share, basic	$ **(0.24)**	$ **(0.13)**	$ **(0.17)**	$ **(0.55)**	$ **(0.21)**
Adjustment for stock-based compensation	0.05	0.09	0.06	0.17	0.25
Adjustment for impairment charges	—	—	0.02	0.02	—
Adjustment for restructuring costs	—	—	—	—	—
Non-GAAP net income (loss) from continuing operations per share, basic	$ **(0.19)**	$ **(0.04)**	$ **(0.09)**	$ **(0.36)**	$ **0.04**
US GAAP net income (loss) from discontinued operations per share, basic	$ **—**	$ **(0.02)**	$ **—**	$ **(0.01)**	$ **(0.04)**
Adjustment for stock-based compensation	—	(0.01)	—	—	0.01
Adjustment for restructuring costs	—	—	—	0.01	—
Non-GAAP net income (loss) from discontinued operations per share, basic	$ **—**	$ **(0.03)**	$ **—**	$ **—**	$ (0.03)
Non-GAAP net income (loss) per share, basic	$ **(0.19)**	$ **(0.07)**	$ **(0.09)**	$ **(0.36)**	$ **0.01**
US GAAP net income (loss) from continuing operations per share, diluted	$ **(0.24)**	$ **(0.13)**	$ **(0.17)**	$ **(0.55)**	$ **(0.21)**
Adjustment for stock-based compensation	0.05	0.09	0.06	0.17	0.25
Adjustment for impairment charges	—	—	0.02	0.02	—
Adjustment for restructuring costs	—	—	—	—	—
Non-GAAP net income (loss) from continuing operations per share, diluted	$ **(0.19)**	$ **(0.04)**	$ **(0.09)**	$ **(0.36)**	$ **0.04**
US GAAP net income (loss) from discontinued operations per share, diluted	$ **—**	$ **(0.02)**	$ **(0.00)**	$ **(0.01)**	$ **(0.04)**
Adjustment for stock-based compensation	—	(0.01)	—	—	0.01
Adjustment for restructuring costs	—	—	—	0.01	—
Non-GAAP net income (loss) from discontinued operations per share, diluted	$ **—**	$ **(0.03)**	$ **—**	$ **—**	$ **(0.03)**
Non-GAAP net income (loss) per share, diluted	$ **(0.19)**	$ **(0.07)**	$ **(0.09)**	$ **(0.36)**	$ **0.01**
US GAAP gross margin percentage from continuing operations	**(23.3)%**	**59.1%**	**25.9%**	**23.5%**	**61.1%**
Adjustment for stock-based compensation included in cost of revenue	11.4%	5.6%	5.1%	5.8%	4.8%
Non-GAAP gross margin percentage from continuing operations	**(11.9)%**	**64.7%**	**31.0%**	**29.3%**	**65.9%**

QUICKLOGIC CORPORATION
SUPPLEMENTAL DATA
(Unaudited)

	Percentage of Revenue			Change in Revenue	
	Q3 2025	Q3 2024	Q2 2025	Q3 2025 to Q3 2024	Q3 2025 to Q2 2025
COMPOSITION OF REVENUE					
Revenue by product: [1]					
New products	47%	81%	79%	(73)%	(67)%
Mature products	53%	17%	21%	46%	40%
Discontinued Operations:					
New products	—%	2%	—%	(100)%	—%
Revenue by geography:					
Asia Pacific	47%	12%	17%	88%	50%
North America	51%	85%	80%	(71)%	(65)%
Europe	2%	2%	3%	(61)%	(64)%
Discontinued Operations:					
Asia Pacific	—%	—%	—%	(100)%	—%
North America	—%	1%	—%	(100)%	—%
Europe	—%	—%	—%	—%	—%

[1] New products include all products manufactured on 180 nanometer or smaller semiconductor processes, eFPGA IP intellectual property, professional services, and QuickAI and SensiML AI software as a service (SaaS) revenue. Mature products include all products produced on semiconductor processes larger than 180 nanometer and includes related royalty revenue.

QuickLogic Corp.

Third Quarter Fiscal 2025 Earnings Results Conference Call

11 November 2025

C O R P O R A T E P A R T I C I P A N T S

Alison Ziegler, *Darrow Associates – Investor Relations*

Brian Faith, *President and Chief Executive Officer*

Elias Nader, *Senior Vice President of Finance and Chief Financial Officer*

C O N F E R E N C E C A L L P A R T I C I P A N T S

Neil Young, *Needham & Company*

Richard Shannon, *Craig-Hallum Capital Group*

Richard Neaton, *Rivershore Investment Research Inc.*

P R E S E N T A T I O N

Operator

Ladies and gentlemen, good afternoon. At this time, I would like to welcome everyone to QuickLogic Corporation's Third Quarter Fiscal 2025 Earnings Results Conference Call.

As a reminder, today's call is being recorded for replay purposes through November 18, 2025.

I would now like to turn the conference over to Ms. Alison Ziegler of Darrow Associates. Ms. Ziegler, please go ahead.

Alison Ziegler

Thank you, Vaughn, and thanks to all of you for joining us. Our speakers today are Brian Faith, President and Chief Executive Officer, and Elias Nader, Senior Vice President and Chief Financial Officer.

As a reminder, some of the comments QuickLogic makes today are forward-looking statements that involve risks and uncertainties, including, but not limited to: statements regarding our future profitability and cash flows; expectations regarding our future business and statements regarding the timing, milestones and payments related to our government contracts; statements regarding the use of the Company's ATM program; and statements regarding our ability to successfully exit SensiML.

Actual results may differ due to a variety of factors including: delays in the market acceptance of the Company's new products; the ability to convert design opportunities into customer revenue; our ability to replace revenue from end-of-life products; the level and timing of customer design activity; the market acceptance of our customers' products; the risk that new orders may not result in future revenue; our ability to introduce and produce new products based on advanced wafer technology on a timely basis; our ability to adequately market the low power, competitive pricing and short time-to-market of our new products; intense competition by competitors; our ability to hire and retain qualified personnel; changes in demand or supply; general economic conditions; political events, international trade disputes, natural disasters and other business interruptions that could disrupt supply or delivery of, or demand of the Company's products; and changes in tax rates and exposure to additional tax liabilities.

For more detailed discussions on the risks, uncertainties and assumptions that could result in these differences, please refer to the risk factors discussed in QuickLogic's most recently filed periodic reports with the SEC. QuickLogic assumes no obligation to update any forward-looking statements or information, which speak as of the respective dates of any new information or future events.

In today's call, we will be reporting non-GAAP financial measures. You may refer to the earnings release we issued today for a detailed reconciliation of our GAAP to non-GAAP results and other financial statements. We have also posted an updated financial table on our IR web page that provides current and historical non-GAAP data.

Please note, QuickLogic uses its website, the Company blog, corporate Twitter account, Facebook page and LinkedIn page as channels of distribution of information about its business. Such information may be deemed material information and QuickLogic may use these channels to comply with its disclosure obligations under Regulation FD.

A copy of the prepared remarks made on today's call will be posted on QuickLogic's IR web page shortly after the conclusion of today's earnings call.

I would now like to turn the call over to Brian. Go ahead, Brian.

Brian Faith

Thank you, Alison. Good afternoon everyone and thank you all for joining our third quarter 2025 conference call.

We have made very significant progress since our August conference call. Last quarter I stated that we focused considerable engineering resources to accelerate storefront design wins for our Strategic Rad Hard FPGA and expand our served available market to include very high-density eFPGA Hard IP designs targeting advanced fabrication nodes. I'm proud to say our engineering team has executed beautifully and we are realizing these goals.

We expect to begin recognizing storefront revenue in early 2026 and that it will provide a meaningful contribution to total 2026 revenue.

The interest from large defense industrial-based entities, or DIBS, in the SRH Test Chip we funded is notably higher than I anticipated.

We have significantly expanded our ability to address the lucrative markets for very high-density discrete FPGAs and ASICs that require large blocks of eFPGA. New contracts and engagements are for much larger blocks of eFPGA and on advanced fabrication processes.

The value contribution of eFPGA in customer designs has grown substantially.

Our penetration in commercial market sectors is expanding, and with this progress, the rate of new contract closure is accelerating to the point that license revenue may surpass NRE revenue for the first time this quarter. We believe these trends will accelerate going forward.

Before I get into the tangible data that support these points, I want to take a moment and provide some color for the revenue guidance Elias will share in his presentation. Based on our backlog and forecasts provided to us by our customers, we are targeting total revenue of $6 million for Q4.

The majority of the contracts that support this outlook are already on the books or have been forecasted by customers to be awarded during the coming weeks. However, a contract valued at nearly $3 million for a commercial application targeting an advanced fabrication node has been forecasted by the customer to be awarded late in the quarter. If this contract is awarded on or very near the date forecasted, we will be able to recognize a large portion of that revenue in Q4 and, with that, realize our $6 million objective. We have a very high level of confidence in winning this contract, but note that it could push into Q1 2026, and that would result in lower Q4 2025 total revenue. Due to this, Elias will present an unusually wide guidance range.

And now, let's walk through our accomplishments.

In early August, we delivered design files to GlobalFoundries to fabricate our SRH FPGA test chip using its 12LP process. This test chip was designed to meet the requirements of certain large DIBs that have programs in development today that are good candidates for this device. We expect delivery of test chips in early Q1 2026 and believe we will have our SRH Dev Kit ready for shipment to customers shortly thereafter.

This initiative was financed by QuickLogic and is independent from our contract with the U.S. Government. Our decision to invest the money and resources to develop this test chip was based on our belief that it is critical in our quest to secure strategic design wins and accelerate our storefront business model.

Since our last earnings conference call, I have personally met with a number of the DIBs that worked with us through the development process, and I cannot emphasize enough the potential of our SRH storefront initiative. In prior meetings all I had to show were PowerPoint presentations, and now with a test chip in fabrication the level of enthusiasm is palpably higher. As a matter of fact, we already have commitments for SRH Dev Kit orders that we expect to receive by the end of this month. I see this as our first tangible step towards the hundreds of millions of dollars in potential Storefront business we could win in the coming years.

The importance of demonstrating our SRH FPGA test chip goes well beyond the storefront designs we believe it will enable us to secure. FPGA is the number one spend category for semiconductor devices by the defense industrial base and custom ASICs are a close second. Together, we believe these two categories make up roughly half of the DIB semiconductor TAM.

We expect many of the new strategic designs that require various levels of radiation hardness will use either discrete FPGA devices that we can storefront or eFPGA Hard IP we can license in new ASIC designs. By delivering a discrete SRH FPGA test chip fabricated on the 12LP process, we are demonstrating the broader capability of our eFPGA Hard IP for ASIC applications that will meet program requirements ranging from radiation tolerant to Strategic Rad Hard.

There are three very important points I want to highlight here. First, DIBs are already using GlobalFoundries' 12LP fabrication process for radiation tolerant and SRH ASICs.

Second, Government contracts require the use of onshore fabrication for strategic programs when devices are available. As it stands today, we will be the only source for Strategic Rad Hard FPGAs and SRH eFPGA Hard IP that is fabricated in the U.S. by a U.S. company.

Third, in my meetings at large DIBs, engineering managers have clearly stated that being able to design with our Aurora FPGA user tools for both our SRH discrete FPGAs and our eFPGA Hard IP in ASIC designs is a huge plus.

During our last conference call I stated that Q3 would mark the low point for revenue recognition for our U.S. Government SRH FPGA contract this year. Funded by the current tranche, revenue recognition from the contract will rebound significantly in Q4. Beyond that, we anticipate an increase in quarterly revenue recognition in 2026 that will be funded by the next tranche.

During our last conference call, I forecasted the award of a mid-seven-figure contract from a DIB during Q4 that targets Intel 18A. Unfortunately, there has been a delay in funding that pushes this contract into 2026. We are highly confident that we'll be awarded this contract, but at this juncture, our customer has limited visibility on the timing of funding. While we await funding for this seven-figure deal, it is worth noting that we have already been awarded multiple contracts by this strategic customer during 2025.

We delivered customer-specific eFPGA Hard IP for this customer's first Intel 18A test chip last April. We expect to receive our allocation of test chips from this contract during Q1 2026 for our internal verification and characterization.

We were subsequently awarded a mid-six-figure contract for a second Intel 18A test chip. We delivered customer-specific eFPGA Hard IP for this test chip during Q3.

In addition to these Intel 18A test chip contracts, during our last conference call, I announced this customer awarded us a contract for a 1 million LUT feasibility study that we are scheduled to deliver next week. We are anticipating a follow-on order in the coming weeks associated with this feasibility study that will enable the customer to tape out a very high density Intel 18A proof of concept device during the second half of 2026.

The architectural changes we implemented in this feasibility study can be leveraged across all advanced fabrication nodes, which we define as 12 nanometers and below. With these changes we can now address the lucrative markets that require very high-density eFPGA blocks in ASIC designs and very high-density discrete FPGAs. This significantly expands our SAM for eFPGA Hard IP and discrete devices, including our SRH FPGA, chiplets and other storefront opportunities.

We initiated our digital proof-of-concept chiplet program earlier this year as a strategy to accelerate our storefront chiplet initiative. Internally, we refer to this as PoC. With the support of our large strategic partners, we have leveraged our existing eFPGA Hard IP and readily available 3rd party IP to move forward rapidly and with minimal investment.

In line with the forecast I shared in our last conference call, we completed the initial phase of the Digital FPGA chiplet PoC, where the eFPGA IP is connected to UCIe IP and the necessary interface logic for the IPs to communicate. This digital simulation of the PoC is available now and can be further developed to meet different customer requirements. Together with our ecosystem partners, we are engaging with prospective customers in the defense, aerospace, industrial and commercial markets.

We plan to move forward with the next phases of the FPGA chiplet PoC once external funding is committed. This phase will include incorporating additional IP such as programmable GPIOs, AXI bus, DSPs, data converters and interfaces such as PCI Express, to meet specific customer requirements. We are optimistic that our PoC initiative will lead to storefront revenue in 2026.

On October 2, we announced a new $1 million eFPGA Hard IP contract for a high performance data center ASIC that will be fabricated on TSMC's 12-nanometer process. In this ASIC, our eFPGA Hard IP will be the primary IP in the design.

This contract is a great illustration of our success in several of the points I mentioned earlier: the need for larger blocks of eFPGA; the increasing value contribution of eFPGA in customer designs; winning contracts for designs targeting advanced fabrication processes, and our growing success in commercial market sectors

We will soon announce the expansion of our involvement with a DIB that specializes in cybersecurity for strategic and tactical weapons systems. This DIB designs secure System-on-a-Chip processors that leverage the enhanced security that only eFPGA can provide. Running these processes in hardware is inherently more secure than software solutions. With eFPGA at the heart of the designs, the hardware can be altered to respond to new threats and updated algorithms. We are proud to have been chosen as a trusted supplier of eFPGA Hard IP for these designs.

Last April, we announced an eFPGA Hard IP contract with a new defense industrial base customer valued at $1.1 million that will be fabricated on the GF 12LP process. This application utilizes a large block of our eFPGA Hard IP for critical functions, which is a trend we are seeing, particularly in designs targeting advanced fabrication nodes. With the cooperation of this DIB and its end-customer, we are leveraging the large eFPGA core into a new seven-figure contract we expect to announce in the coming weeks.

In the scope of this new contract, we will be provided with test chips that we will incorporate in an evaluation kit. The evaluation kit will be compatible with common third-party development environments used by both DIBs and commercial customers. This enables these customers to accelerate system level evaluations and designs that can use either a storefront version of the 12LP test chip or our eFPGA Hard IP in an ASIC. We anticipate having evaluation kits available in late 2026.

With that, I will turn the call over to Elias for his presentation of financial data.

Elias Nader

Thank you, Brian and good afternoon, everyone.

Total third quarter revenue was $2 million and aligned with the midpoint of our guidance. Total revenue was down 52.5% from Q3 2024 and down 45% compared to Q2 2025.

Rounded to the nearest $100,000, new product revenue in Q3 was $1 million and mature product revenue was $1.1 million. New product revenue was down 73.1% from Q3 2024 and down 67.3% compared to Q2 2025. Mature product revenue was up from $0.7 million in the third quarter of 2024 and up from $0.8 million in the second quarter of 2025.

Non-GAAP gross margin in Q3 was a negative 11.9%. This compared with non-GAAP gross margin of 65.3% in Q3 2024 and 31% in Q2 2025. The primary reasons for the lower Q3 gross profit margin are unfavorable absorption of fixed costs due to lower revenue and the fact that $300,000 of R&D costs were allocated to COGs.

Non-GAAP operating expenses in Q3 were approximately $2.9 million. This was approximately $300,000 below the mid-point of our outlook due to the COGS allocation I just mentioned. This compares with non-GAAP operating expenses of $3.3 million in the third quarter of 2024 and $2.5 million in the second quarter of 2025.

Non-GAAP net loss was $3.2 million, or $0.19 cents per diluted share. This compares to non-GAAP net loss of $0.9 million, or $0.06 per diluted share in Q3 2024, and a non-GAAP net loss of $1.5 million, or $0.09 cents per diluted share in the second quarter of fiscal 2025.

The difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses, impairment charges and restructuring costs. Stock-based compensation for Q3 was $0.8 million. Stock-based compensation was $1.2 million in Q3 2024 and $0.8 million in Q2 2025. Impairment charges were $0.3 million in Q2 2025.

For the third quarter, three customers accounted for 10% or more of total revenue.

At the close of Q3, total cash was $17.3 million, inclusive of utilization of $15 million from our $20 million credit facility. This compares with $19.2 million inclusive of usage of $15 million from our $20 million credit facility at the close of Q2 2025.

Net of approximately $200,000 raised with our ATM in July, cash usage during Q3 was approximately $1.9 million. This was primarily driven by tape-out and wafer costs associated with our internally financed SRH FPGA test chip. In addition to these one-time costs, there were also expenditures related to revenue contracts and repayments for financed tooling and equipment.

Now, moving to our guidance and outlook for our fiscal fourth quarter, which will end on December 28, 2025, based on backlog and customer forecasts we are targeting total revenue of $6 million for Q4. Many of the contracts that support this outlook are already on the books or have been forecasted by customers to be awarded during the coming weeks. However, the customer for a contract valued at nearly $3 million for a commercial application has forecasted the award late in the quarter. If this contract is awarded on or very near the date forecasted, we will be able to recognize a large portion of that revenue in Q4, and with that, realize our $6 million objective. We have a very high level of confidence in winning this contract but note that it could push into Q1 2026 and that would result in Q4 revenue of $3.5 million. Due to this, our guidance range for total Q4 revenue is $3.5 million to $6 million. At $3.5 million, we expect total revenue to be comprised of $2.5 million in new product revenue and $1 million in mature product revenue. At $6 million, we expect $5 million in new product revenue.

Based on the anticipated Q4 revenue mix, non-GAAP gross margin for the fourth quarter is expected to be approximately 45% at $3.5 million of revenue and 68% at $6 million of revenue. At the low end of the range, the primary reason for a lower gross profit margin is attributed to less favorable absorption of fixed costs.

Taking the range of our Q4 outlook into consideration, our full-year 2025 non-GAAP gross profit margin is expected to be 38% plus or minus 5%.

Our Q4 non-GAAP operating expenses are expected to be approximately $3 million, plus or minus 5%. With this, we are modeling full year 2025 non-GAAP OpEx will be approximately $11.3 million.

Please note that given the nature of our industry, we may occasionally need to classify certain expenses to COGS versus OpEx or capitalize certain costs. These classifications are related to labor and tooling for our IP contracts with customers. This may cause variability in our quarterly gross margins and operating results that will usually balance out on the operating line.

After interest and other income, at the low end of the revenue range we forecast a Q4 non-GAAP net loss of approximately $1.9 million or $0.11 per share. At the high end of our revenue range, we are projecting a non-GAAP net profit of approximately $600,000 or $0.04 per share.

The main difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses. In Q4, we expect this compensation will be approximately $800,000. This is the same as Q3 2025 and down slightly from Q4 2024. As a reminder, there will be movement in our stock-based compensation during the year, and it may vary each quarter based on the timing of grants.

Even at the low end of our revenue guidance range, we anticipate positive cash flow in Q4. However, the timing of payments from our U.S. Government contract could negatively impact this outlook. Given the fact we raised approximately $2 million using our existing ATM in October, we are well prepared for any delayed payments associated with the U.S. Government contract.

Thank you. With that, let me now turn the call over to Brian for his closing remarks.

Brian Faith

Thank you, Elias. We have logged considerable progress during the last few months and we are leveraging that progress to produce tangible results. Earlier I talked about those results and now I would like to take the next few minutes to help you understand the industry trends that are driving these results. With that understanding, I think you will appreciate what is driving the increased interest in FPGA technology and why more companies are incorporating larger blocks of eFPGA at the core of new ASIC designs.

The overarching trend in both commercial and DIB designs is smart systems. Smart systems rely on algorithms for their intelligence. Algorithms can be processed much faster and with much lower power consumption in hardware than software. Hardware processing is also inherently more secure against cyber threats than software.

The challenge here is that algorithms must be updated over the lifecycle of the product. This means hardware must be programmable so it can adapt to changing algorithms. This has led to the need for larger blocks of eFPGA at the heart of ASIC designs versus past use cases where small blocks of eFPGA were more commonly used as programmable connectivity bridges. This means both the need and the value proposition for eFPGA are increasing.

Sophisticated smart systems designs typically target advanced fabrication nodes. This means higher fixed costs and longer design cycles for ASICs. To favorably offset these higher fixed costs, ASIC designs must deliver longer lifecycles than in the past. Designs that employ eFPGA can adapt to changing algorithms, evolving functional requirements and external changes that are not evident during the design cycle. This flexibility lengthens the lifecycle of ASIC designs and provides program managers with the confidence to move ASICs to production more quickly and with lower risk. This shortens design cycles and lowers development costs.

Last, but certainly not least, there are many programs in development today that must be compliant with rigorous environmental requirements ranging from Radiation Tolerant to Strategic Rad Hard. Our internally funded development of an SRH FPGA test chip is designed to address the full range of these requirements and accelerates our ability to pursue design wins.

By using the same onshore 12LP fabrication process that DIBs have used for SRH ASICs, we are optimizing our chances of winning discrete FPGA designs we can storefront and contracts for eFPGA Hard IP that customers can incorporate in ASIC designs. Further enhancing our position is the fact customers can execute designs with our Aurora user tools for both.

The fact this investment by QuickLogic has been received very well by strategic DIBs is underscored by the commitment we have for SRH Dev Kit orders that we anticipate receiving by the end of this month.

Before I turn the call over for Q&A, I want to take a moment to recognize Veterans Day and express my heartfelt gratitude to all those who have served our country. This day has personal meaning for me as several members of my family have served and I have deep respect for the sacrifices made by veterans and their families. It's something we honor at QuickLogic, especially as we develop technologies that contribute to our nation's defense and security.

Operator, I would now like to open the call for questions.

Operator

Thank you. We will now be conducting a question-and-answer session where selected analysts will be invited for questions. If you would like to ask a question, please press star, one on your telephone keypad. A confirmation tone will indicate your line is in the question queue. You may press star, two if you would like to remove your question from the queue. For participants using speaker equipment, it may be necessary to pick up your handset before pressing the star keys..

Our first question comes from Quinn Bolton with Needham. You may proceed with your question.

Neil Young

Hey everyone. It's Neil Young on for Quinn Bolton. Thank you for letting me ask a question. Like I said, on for Quinn. Sorry about that.

What impact is the government shutdown having on your business? Based on the prepared remarks it sounds like you've seen some delays of projects. Have you seen any cancellations? Then, given the ongoing shutdown, although it is allegedly supposed to end soon here, what gives you confidence in a rebound of the USG Strategic Radiation Hard and FPGA program in 4Q? And then I have a follow-up. Thanks.

Brian Faith

I think firstly, let's zoom out. Programmable logic has been a big part of the defense industrial base for decades and that's not changing. It's pervasive across 75% of defense systems, and as I mentioned earlier, a very large percentage of the total semiconductor spend by the DOD, so that demand is not going away.
The question is, as you get down to the nuts-and-bolts of these programs, is the funding going to be there based on the budgets and whatnot?

So I think that from the programs that we have today on contract, we're not seeing any delays with those. Elias did mention in his conversation about the cash usage for the quarter, or I should say net cash gain in the quarter, we did use the ATM in October sort of as an anticipation in case there was something like this that happened as far as funding goes. So if there's a delay in funding, then we have no issue with that. If there's no delay, then we'll have a good positive cash flow for the quarter.

Aside from that, if you look at other contracts coming down the pipe, I mean, you could find this all publicly that a lot of the new RFIs or RFSs or RFPs that were coming out from the government for various development programs, some of those were actually paused, and I think that's largely because some of those workers that were driving that were put on furlough. Again, I don't anticipate those going away permanently. It's more once the government is funded and people get back from furlough, these are going to be full steam ahead. So you might see a delay in some of those new programs, but not the ones that we're fully executing on today. I just don't see that change because this is not an experimental technology.
There are actual programs of record that need this today and moving forward on that.

Does that answer your first question?

Neil Young

Yes, very helpful. Thank you. Then the second question I wanted to ask, so it sounds like storefront revenue in 2026 is supposed to have a meaningful step up. If possible, I was wondering if you could maybe size the range of storefront revenue you think is possible, and then, you know, if not, maybe you could give us some idea of what could drive upside to your internal expectations or on the other side, perhaps, drive downside to those expectations. Thanks.

Brian Faith

Sure. I'll start with the what and then I'll answer with the why.

So on the what side, I would say significant for us is going to be the 10% or thereabouts of total revenue. Without giving the exact number because we haven't put numbers out for 2026 yet, we think that the storefront revenue associated with these developments that we've been talking about is going to be meaningful, meaning it'll be in that 10% range. And yes, I do think next year's revenue will be notably higher than this year's total revenue.

As you get into why do I feel like that, I think if you go back to my opening remarks about the Strategic Rad Hard Initiative, I cannot tell you how many meetings I've had in the last quarter since the last conference call face-to-face with these DIBs that see what we're doing, they like the fact that we've done this tape out that we talked about, and, you know, even as of today, lots of calls and emails asking for when they can get their hands on this. So when you start to see people pulling for the technology and you know the projects that are under development—public projects, right? The strategic defense system is going under a major modernization. That's all public knowledge. And then if you throw into that this notion of hypersonics and Golden Dome, a lot of these programs are going to need some level from Strategic Rad Hard down to Radiation Tolerant, and the part that we've got in the fab now is designed to address those needs.

So as we get it out, we start moving to these orders for dev kits, we start getting those out. Hopefully by the end of Q1, I think we're going to be in a real prime spot to monetize that and start turning talk that I've had for two and a half years into actual revenue and bottom line contribution.

But it's not just one entity here. We're talking about all the major DIBS that we've been talking to, I think there's good demand for that. That's why we think it's going to be meaningful for next year.

Does that answer your question?

Neil Young

Thank you. Yes. Thank you very much.

Brian Faith

Great. You're welcome.

Operator

Our next question comes from Richard Shannon with Craig-Hallum. You may proceed with your question.

Richard Shannon

Great. Thanks, Brian and Elias, for taking my questions. The quality of the audio here is pretty poor on my end, so hopefully you can hear me. I apologize if you can't hear.

Brian Faith

We can hear you just fine.

Richard Shannon

Okay. Well, let's good. I guess at least one of us can.

A lot of detail on the call here and some really interesting stuff going on here. Let me ask kind of a big-picture, high-level question here with your new initiative on the GF 12LP process or initiative here. I guess how do we think about the opportunity for FPGAs versus ASICs? It would include your Hard IP in here. Are the dynamics here for timing for each of these markedly different than the other?

Brian Faith

Well, I'd start by saying for 12LP, that is a very commonly used process by the defense industrial base. I think the heritage of that is that that was the most advanced process that GlobalFoundries had and GlobalFoundries is U.S.-owned and operated, and so if you wanted to have something that was manufactured onshore by a U.S. company, that was sort of the most advanced you can get.

Global has since come out with 12LP+, which is a more advanced version of 12LP. But if you think about what's involved in doing an ASIC or an SOC, you need lots of IP available and you need lots of test data characterization on all that IP in order to feel comfortable to move forward with that on your ASIC.

In terms of the defense community, it's a very risk-averse community, as they should be as they're designing these systems. So there's a wealth of IP on 12LP that there is, it's today, it’s known, it’s understood characterization data. And the government—again, this is all publicly findable. The government has been helping people do ASICs on 12LP. A lot of IP is available. There's government-funded multi-project wafers and all those things to encourage development on that node.

So from that standpoint, I think you're going to see 12LP a lot. You've seen it in the past. You're going to see it in the future.

So then the question for us is, okay, we have our IP on 12LP. Now we can build devices from that or we could license that for people doing their own ASICs. I think we've already talked about IP licenses that we have on ASICs, and you've heard timing on that. So people will start to be taping up those and going to production, hopefully, in the next few years. So, there’s a near-term license opportunity, there’s a back end royalty opportunity for us on that. And we definitely plan to monetize that to several million dollars a year.

On the device side, that gets interesting because we've obviously taken our commercial 12LP IP and we've done a Rad Hard implementation of that. The goal behind that is to do this strategic Rad Hard FPGA and having—take that out, if you fast-forward to when we could do that actual product dive for production on that, once that's out that's going to be a significant step-function increase in the revenue potential for us personally, because devices of that nature are always going to have a much higher ASP than what a royalty contribution would be.

So I think 12LP is critically important for us and it's sort of a land and expand strategy on that now where we want to license it to as many people as we can. We want to have this strategic Rad Hard FPGA capture for revenue, and that's I think the basis of what could be hundreds of millions of dollars in revenue.

I don't know if I answered your question in its entirety. If I didn't, just tell me.

Richard Shannon

You did for the most part. I'm just trying to circle around this a bit here from a very high level. I'm going to ask another pretty high-level question here, Brian, which is comparing the opportunity you've now undergone with GFS 12LP, how do you compare the opportunity to what you've been doing with Rad Hard with the other founders you've announced with? I guess from a total perspective —I'll let you pick a timeframe, but how do you see the relative size of each of these opportunities?

Brian Faith

By the other funders, you're referring to Skywater and Honeywell or somebody else?

Richard Shannon

Those are the ones, yes.

Brian Faith

Okay. So I think, without getting into programmatic details, I think that the 12LP opportunity for us is a larger opportunity because it has the strategic Rad Hard FPGA. It also has IP licensing as an option. And one of the nice things—and you know this—is that as you get smaller process technology, you get denser transistors, you get more capability, you can stuff in a die, and there's going to be higher value to that. We enumerate that as far as where we're taking our eFPG architecture, but the same is true with 12-nanometer and 12LP. The more transistors and functionality we can stick on that die, the higher the value the part's going to be.

I think, again, the interesting part about 12LP here is that we can get a lot of capability running on our FPGA 12LP, and maybe somebody doesn't even need to do an ASIC now for 12LP. That's huge. If we can start helping people address the needs of a mission without having to go off and do a custom ASIC, you're talking about saving a customer, the government, literally tens of millions of dollars in years of development cost and time. That's the real benefit, I think, to getting our FPGA on 12-nanometer, given that it's strategic Rad Hard and still capable of the node.

Now, as you talk about those other foundries, those are older process geometries that they've talked about and so there's going to be a difference in what you can do on the die. There's a difference in what you can do capability-wise. Not bad, just different. But I think the bigger bucket of revenue for us is going to be what we're going to be able to do with 12-nanometer on these for the time being.

I don't want to get into more details on that just because that's a little too much programmatic information if I go further.

Richard Shannon

Yes, I get that. Just that high level here is very helpful to think about, Brian. Thanks for that.

You mentioned expecting orders for your new dev kits here, I think, by the end of this month and delivering those sometime next year. Can you give us a sense of how many dev kits and how many customers you expect to ship that to? Then what's kind of the design cycle once customers get that in hand in terms of their next steps?

Brian Faith

So, I'm not going to give numbers. You're probably not surprised to hear that. But it's going to be enough that it will be a significant revenue number, so not just a rounding number on the income statement. Elias talked about the money that we spent in Q3 on that. We've intentionally bought enough die that we can provide enough for these customers that want to test these things out, both in terms of dev kit and on just raw devices themselves on their own boards.

Now, the way this works from an evaluation perspective, again, this is a very cautious and risk-averse community that we're talking about. They're going to want to do their own testing on these things, and that generally takes a couple quarters to go off and do all of your exercising of your design and the different environmental tests that need to be done on those devices. You've probably read the TRL levels, technology readiness level. You know, we want to get customers as quickly as possible to TRL 5. TRL 5 is where they can actually say that they've taken the part and they've run it through the rigorous testing that's representative of the environment that they're going to operate in. We hope to be able to support our customers to get through that at some point through the middle of next year, and then at that point start intercepting actual programs of record with this and moving into pretty late stages of the design hopefully with them.

Again, that's why time is so critical. That's why we took the leap of faith to do their own design and fund our own tape out, knowing that MPWs (phon) don't come along very often, and we wanted to make sure that we're on one that still gave us enough time to have the part come out, verify it, and get it into the hands of the dev so they can start playing with it in their own labs and not just trust our own data.

Richard Shannon

Okay. Great perspective there, Brian. Last question, I'll jump out of line.

A lot of irons in the fire that you have going on here, which is great to see here. And QuickLogic, obviously, is a fairly small company here. Seems like it might need a bit more support to a broad range of customers coming your way here very soon.

How do we think about the spend levels we need to see next year, whether it comes through OpEx or the stuff that gets allocated to COGS here? How do we think about where this could go if things go really well and you get a lot of attention. A lot of activity these dev kits are sending out?

Brian Faith

So I'll start, answer, and Elias can chime in on this. From the engineering perspective and the go-to-market team perspective, we obviously have identified certain critical hires. Some of them you can find on our website today. These are all about getting the right resources to get the devices out into the hands of the DIBs as soon as possible. You can find that on our website. Engineering, field application engineering, and so on.

As we move from test chip to actual product chip, there will be more expenses. There will be other things that need to be paid for. I think that we have a good line of sight on what those are going to be. And it's not going to be outrageous for next year. I think it's going to be very mindful of where we are financially as a company and tied in with getting these customers on board with test chips so that any investments we do make, it's coming from the perspective of knowing what our customer wants, knowing the problem that our solution solves, and in some cases, even perhaps getting funding from customers to co-invest in these things so that they have skin in the game and it offsets the upfront cost for QuickLogic to get it to market.

Elias Nader

Yes, correct. In fact, Richard, if I may add, like for example, we have three new hires we're looking for, all engineers. As such, you know, OpEx is definitely headcount moderating, so I don't anticipate—even with all the additions that Brian is describing, probably we'll be looking at probably $3.5 million of OpEx per quarter probably next year but starting in Q2 or so. I think for now we're okay with about under three.

Richard Shannon

Okay. That's great detail, guys. I will jump the line. Thank you.

Brian Faith

Thanks, Richard.

Operator

Before our next question, as a reminder, if any analyst would like to ask a question, you may press star. One on your telephone keypad to enter the queue.

Our next question comes from Rick Neaton with Rivershore Investment Research. You may proceed with your question.

Richard Neaton

Thank you. Hi, Brian, and hi, Elias.

Elias Nader

Hello, Rick.

Richard Neaton

I'd like to understand your Q4 guidance. Are you proposing a either/or situation where we're either going to have $3.5 million plus or minus or $6 million plus or minus? Is that what you're saying?

Elias Nader

Yes, because there's an issue with timing, right? So if the order comes in, for example, to complete it to six million, it would come in late in the quarter. We may be able to recognize certain portions of that revenue.

But if it comes in and we're not able to deliver in that quarter—let's just say it comes in on the day of our close or the day after, it's definitely Q1 at that point. So it's almost like a timing issue, Rick. That's why we went to great pains to identify the difference between a $3.5 million revenue and $6 million revenue, and really it's one order. And as such, it's all about timing.

It’s very difficult to answer a question now to someone saying, okay, would you be able to recognize 100% of it? And the answer is clearly no, if it comes in in Q4. So that is why Brian and I agreed. If that's the case, and we anticipate that order coming in, at least in Q4—let's just hope it does—we at least have the possibility of beating the high end of the range.

Richard Neaton

Okay. Thank you for that explanation.

Elias Nader

Sure.

Richard Neaton

What do you forecast as your share count for 2025?

Elias Nader

Well, 17,952,000 shares, that's outstanding right now.

Richard Neaton

Okay. One final question. That’s fine. So that's your ending share count would be 17 million?

Elias Nader

Yes, sir.

Richard Neaton

Okay. Three months ago, you described your expected revenue decline for 2025 with the adjective modest, and now your Q4 guidance suggests a 20% to 30% decline in annual revenue from 2024. What changed since August to cause what I would describe as a significant double-digit percentage-wise revenue decline?

Brian Faith

Rick, that's the challenge with having large IP contract values. When we're talking $3 million type ASPs for these. I think in the call, we mentioned one clearly is in 2026, so that goes from this year into next year, and then some other smaller ones that contribute to that. But again, when you have $3 million IP contracts, if they don't happen in the year, the fiscal year, there's going to be a big change in percentage-wise from the revenue levels that we're at today.

Once that becomes more of the norm, and we get more of these higher value contracts like we're talking about now, that starts to smooth out some of that lumpiness. But when we're at the stage where we are now, there's almost unavoidable if something goes out that's going to materially impact the percentage of that.

Richard Neaton

Okay. Thanks for that explanation and thanks for having me on the call.

Brian Faith

Thanks, Rick.

Operator

This now concludes our question and answer session. I would like to turn the floor back over to Brian Faith for closing comment.

Brian Faith

I want to thank everybody for joining us today. Hopefully, we'll connect with some of you at one of our upcoming events, including the Craig-Hallum Alpha Select 101 Conference in New York on November 18, the Semiconductor-Focused Annual New York Summit, also in New York on December 16, or the Annual Needham Growth Conference in early January 2026. Thank you and have a good day.

Operator

Ladies and gentlemen, thank you for your participation. This does conclude today's teleconference. Please disconnect your lines and have a wonderful day.