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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C. 20549

FORM 10-K

<TABLE>
<C> <S>
/X/ ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 FOR THE FISCAL YEAR ENDED: DECEMBER 31, 1999
</TABLE>

OR

<TABLE>
<C> <S>
/ / TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
</TABLE>

FOR THE TRANSITION PERIOD FROM _____ TO _____

COMMISSION FILE NUMBER: 000-22671

QUICKLOGIC CORPORATION
(Exact name of registrant as specified in its charter)

<TABLE>
<S> <C>

DELAWARE	77-0188504
(State or other jurisdiction of incorporation or organization)	(I.R.S. Employer Identification Number)
1277 ORLEANS DRIVE SUNNYVALE, CA	94089
(address of principal executive offices)	(zip code)

</TABLE>

Registrant's telephone number, including area code: (408) 990-4000

SECURITIES REGISTERED PURSUANT TO SECTION 12(b) OF THE ACT: None

SECURITIES REGISTERED PURSUANT TO SECTION 12(g) OF THE ACT: Common Stock, $0.001 par value

(Title of Class)

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes /X/ No / /

Indicate by check mark if disclosure of delinquent filers pursuant to item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. / /

The aggregate market value of voting stock held by non-affiliates of the registrant as of March 27, 2000, was $443,928,836.40 based upon the last sales price reported for such date on The Nasdaq National Market. For purposes of this disclosure, shares of Common Stock held by persons who hold more than 5% of the outstanding shares of Common Stock and shares held by officers and directors of the registrant, have been excluded in that such persons may be deemed to be

affiliates. This determination is not necessarily conclusive.

At March 27, 2000 Registrant had outstanding 18,160,330 shares of Common Stock.

DOCUMENTS INCORPORATED BY REFERENCE

The Registrant has incorporated by reference into Part III of this Form 10-K portions of its Proxy Statement for Registrant's Annual Meeting of Stockholders to be held on or about May 31, 2000.

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EXPLANATORY NOTE

THIS ANNUAL REPORT ON FORM 10-K CONTAINS CERTAIN FORWARD-LOOKING STATEMENTS (WITHIN THE MEANING OF SECTION 27A OF THE SECURITIES ACT OF 1933, AS AMENDED, AND SECTION 21E OF THE SECURITIES EXCHANGE ACT OF 1934, AS AMENDED) THAT INVOLVE RISKS AND UNCERTAINTIES. ACTUAL RESULTS AND THE TIMING OF CERTAIN EVENTS COULD DIFFER MATERIALLY FROM THOSE PROJECTED IN THE FORWARD-LOOKING STATEMENTS AS A RESULT OF CERTAIN KNOWN AND UNKNOWN FACTORS, INCLUDING THE RISK FACTORS BEGINNING ON PAGE 27 OF THIS REPORT AND OTHER FACTORS DISCUSSED ELSEWHERE IN THIS ANNUAL REPORT ON FORM 10-K.

PART I

ITEM 1. BUSINESS

OVERVIEW

QuickLogic develops, markets and supports advanced field programmable gate array, or FPGA, semiconductors and the software tools needed for our customers to use our products. In addition to our FPGA semiconductors, we have pioneered the development of embedded standard products, or ESPs. Our ESPs combine the flexibility and time-to-market advantages of our FPGAs with the predictable, high performance of standard semiconductor products, thereby enabling our customers to integrate increased amounts of functionality on a single semiconductor device. Our FPGA and ESP products target complex, high-performance systems in rapidly changing markets where system manufacturers seek to minimize time-to-market and maximize product differentiation and functionality. Examples of markets we sell to include telecommunications and data communications; video/audio, graphics and imaging; instrumentation and test; high-performance computing; and military systems.

The key components of our FPGA and ESP product families are our ViaLink programmable metal technology, our pASIC architecture and the associated software tools used for product design. Our ViaLink technology allows us to create smaller devices than competitors' comparable products, thereby minimizing silicon area and cost. In addition, our ViaLink technology has lower electrical resistance and capacitance than other programmable technologies and, consequently, supports higher signal speed. Our FPGA and ESP architectures provide full routability and utilization of a device's logic cells, thereby enabling greater usable device density and design flexibility. Finally, our software enables our customers to efficiently implement their designs using our products.

INDUSTRY BACKGROUND

Competitive pressures are forcing manufacturers of electronic systems to rapidly bring to market products with improved functionality, higher performance and greater reliability, all at lower cost. Providers of systems requiring high-speed data transmission and processing such as communications equipment, digital image products, test and instrumentation and storage subsystems face some of the most intense time-to-market pressures in the technology industry. These market forces have driven the evolution of logic semiconductors, which are used in complex electronic systems to coordinate the functions of other semiconductors, such as microprocessors or memory. There are three types of advanced logic semiconductors:

- Application Specific Integrated Circuits, or ASICs, are special purpose devices designed for a particular manufacturer's electronic system. These devices are customized during wafer manufacturing.

- Application Specific Standard Products, or ASSPs, are fixed-function devices designed to comply with industry standards that can be used by a variety of electronic systems manufacturers. Their functions are fixed

prior to wafer manufacturing.

- Programmable Logic Devices, or PLDs, are general purpose devices which can be used by a variety of electronic systems manufacturers, and are customized after purchase for a specific application. Field Programmable Gate Arrays, or FPGAs, are types of PLDs used for complex functions.

Systems manufacturers have relied heavily on ASICs to implement the advanced logic required for their products. ASICs provide high performance due to customized circuit design. However, because ASICs are design-specific devices, they require long development and manufacturing cycles, delaying product introductions. In addition, because of the expense associated with the design of ASICs, they are cost effective only if they can be manufactured in high volumes. Finally, once ASICs are manufactured, their functionality cannot be changed to respond to evolving market demands.

ASSPs have become widely utilized as industry standards have developed to address increasing system complexity and the need for communication between systems and system components. These standards include:

- Peripheral Component Interconnect, or PCI, a standard developed to provide a high performance, reliable and cost-effective method of connecting high-speed devices within a system.

- SONET, or Synchronous Optical NETwork, a fiber-optic transmission standard for high-speed digital traffic, employed mainly by telephone companies and other network service providers.

- Ethernet, a widely-used local area network, or LAN, transport standard which controls the interconnection between servers and computers.

- Fibre Channel Interconnect Protocol, an industry networking standard for storage area networks, or SANs, which controls the interconnection between servers and storage devices.

Compared to ASICs, ASSPs offer the systems designer shorter development time, lower risk and reduced development cost. However, ASSPs generally cannot be used by systems manufacturers to differentiate their products.

To address markets where industry standards do not exist or are changing and time-to-market is important, FPGAs are often used. FPGAs provide systems manufacturers with the flexibility to customize and thereby differentiate their systems, unlike ASSPs. FPGAs also enable systems manufacturers to change the logic functionality of their systems after product introduction without the expense and time of redesigning an ASIC. However, most FPGAs are more expensive than ASSPs and even ASICs of equivalent functionality because they require more silicon area. In addition, most FPGAs offer lower performance than nonprogrammable solutions, such as ASSPs and ASICs. According to inSearch Research, the projected total market size for high-complexity programmable logic devices in 2000 is approximately $3.0 billion, of which FPGAs are estimated to account for $1.8 billion.

QUICKLOGIC'S FPGA SOLUTION

QuickLogic's FPGAs offer higher performance at lower overall systems cost than competing FPGA solutions, in addition to offering the advantages typically associated with FPGAs. Specifically, our products provide greater design flexibility than standard FPGAs and enable designers of complex systems to achieve rapid time-to-market with highly differentiated products. Our products are based on our ViaLink technology and pASIC architectures, and our associated QuickWorks and QuickTools design software:

- VIALINK PROGRAMMABLE METAL TECHNOLOGY. Unlike conventional SRAM-based FPGAs, our ViaLink programmable metal technology embeds logic interconnects between the metal layers of a chip, instead of on the silicon substrate. As a result, we are able to provide a programmable switch at every intersection in the wire grid, as illustrated in the graph below. This vertical interconnect structure is more efficient and flexible than that of conventional FPGAs, minimizing silicon area and therefore cost. The ViaLink technology also features lower resistance and capacitance than competing interconnect technologies, thereby optimizing the device's performance.

- PASIC ARCHITECTURE. FPGA device architectures consist of logic cells,

routing wires and interconnect elements. Unlike conventional SRAM-based FPGA architectures, our pASIC architectures facilitate full utilization of a device's logic cells and Input/Output pins. These logic cells have been optimized to efficiently implement a wide range of logic functions at high speed. Our pASIC architectures use our ViaLink technology to maximize interconnects at every routing wire intersection. The abundance of interconnect resources allows more paths between logic cells. As a consequence, system designers are able to use QuickLogic FPGAs with smaller gate counts than competing FPGAs to implement their designs. These smaller gate count FPGAs require less silicon area and as a result are able to be offered at a lower price.

- QUICKWORKS AND QUICKTOOLS DESIGN SOFTWARE. Our design software for Windows and Unix operating systems provides systems manufacturers with the ability to easily customize QuickLogic FPGAs for their specific needs. These design tools feature 100% fully automatic place and route capabilities, which speed design development by permitting very complex designs to be implemented quickly. Once a design has been completed, systems manufacturers can use the DeskFab device programmer to transfer their design to an FGPA in minutes. Alternatively, systems manufacturers can use our unique WebASIC program to transmit their design to QuickLogic in order to receive a programmed device for evaluation within two business days.

THE ADVENT OF SYSTEM-ON-A-CHIP

Over the past few years, semiconductor manufacturers have migrated to smaller process geometries. These smaller process geometries enable more logic elements to be incorporated in a single chip using less silicon area. More recently, advances have been made in the integration of logic and memory on a single chip, which had been difficult previously due to incompatible process technologies. Advantages of the single chip approach to systems manufacturers include:

- simplified system development,

- reduced time-to-market,

- elimination of delays associated with the transfer of data between chips,

- smaller physical size,

- lower power dissipation,

- greater reliability and

- lower cost.

However, as levels of logic integration have increased, devices have become more specific to a particular application. This fact limits their use and potential market size.

QUICKLOGIC'S ESP SOLUTION

QuickLogic has leveraged its unique FPGA technology to address the limitations inherent in current system-on-a-chip approaches. The result is embedded standard products, or ESPs, that deliver the advantages offered by both FPGAs and ASSPs. In its simplest form, an ESP contains four basic parts: a programmable logic array, an embedded standard function, an optional programmable read-only memory to configure the embedded function, and an interface that allows communication between the standard function and programmable logic array. Our ESP products combine the system-level functionality of ASSPs with the flexibility of FPGAs. We believe ESPs offer the following specific advantages:

- INCREASED PERFORMANCE. In a typical design, data must travel between an ASSP and an FPGA across a printed circuit board. The limited number of connections available and the distance between the

devices can degrade the system's overall performance. Our ESP solution allows all data to be processed on a single chip.

- DECREASED COST. Because our ESP is a single chip solution, it requires less silicon area, and therefore is less expensive to produce. Additionally, this single chip approach lowers the component, assembly and test cost for the system manufacturer.

- INCREASED RELIABILITY. ESP designs are more reliable because single chip solutions contain fewer components and circuit board connections that are subject to failure.

- SHORTER DEVELOPMENT TIME. With a multiple chip design, systems designers must solve complex routing and timing issues between devices. A single chip ESP solution eliminates the timing issues between devices and simplifies software simulation, leading to shorter development time.

We have introduced our first two ESP product lines, the QuickRAM and QuickPCI families. We have announced a new product family, QuickDSP, which will be introduced in the second quarter of 2000. All three families are designed for a wide range of performance-driven applications. For example, QuickRAM products, which combine blocks of embedded, high-performance memory with our FPGA logic, are used by Alcatel in its Lightwave telecommunication transmission systems. QuickPCI products combine PCI controllers with our FPGA logic. We completed development of our first QuickPCI product in April 1999, and have made shipments to several customers. QuickDSP products use mathematical functions to modify digital signals in desirable ways.

According to inSearch Research, the total ESP market size in 1999 was $8.0 million, and is projected to increase to $32.0 million in 2000.

THE QUICKLOGIC STRATEGY

Our objective is to be the leading provider of high-speed, flexible, cost-effective FPGAs and ESPs. We feel we can achieve this objective by offering systems manufacturers the ability to accelerate design cycles to satisfy demanding time-to-market requirements. To achieve our objective, we have adopted the following strategies:

EXTEND TECHNOLOGY LEADERSHIP

Our ViaLink technology, pASIC architectures and proprietary software design tools enable us to offer flexible, high-performance FPGA and ESP products. We intend to continue to invest in the development of these technologies and to utilize such developments in future innovations of both our FPGA and our ESP products. We also intend to focus our resources on building critical systems-level expertise to introduce new ESP products and enhance existing ESP product families.

CAPITALIZE ON CROSS-SELLING OPPORTUNITIES BETWEEN OUR FPGA AND ESP PRODUCTS

Because our development tools share many of the same features for both FPGAs and ESPs, once a manufacturer designs a system with either product, we believe the manufacturer will recognize the advantages of our other products. Accordingly, we intend to leverage our FPGA and ESP design wins to pursue additional design wins on complementary products with the same customer.

BROADEN ESP PRODUCT LINES

In addition to our ESP product families, we intend to focus on the needs of large, high-growth, performance-driven market segments. Our product design approach consists of continuous solicitation of feedback from existing and prospective customers.

CREATE INNOVATIVE, INDUSTRY-LEADING CUSTOMER SERVICES

We continue to develop and implement innovative ways to serve and communicate with our customers. For example, we recently introduced our WebASIC service. This service allows our customers to use our development software to design a circuit, transmit design information over the Internet and receive a QuickLogic FPGA or ESP device programmed with their design within one business day in North America and Europe or within two business days in Asia. We are in the process of deploying ProChannel, a web-based system which will allow our customers to obtain promotional material, receive quotations, place orders for our products and view their order status over the Internet. This system will complement the Electronic Data Interchange systems that we have used for the past several years with our largest customers.

TARGET HIGH-PERFORMANCE, RAPIDLY CHANGING MARKETS

We will continue to focus our design and marketing efforts on systems manufacturers who sell complex systems that require high performance, design

flexibility, low cost and rapid time-to-market. Such applications include telecommunications and data communications; video/audio, graphics and imaging systems; instrumentation and test; high-performance computing; and military systems.

MARKETS AND APPLICATIONS

Our FPGA and ESP products are targeted at high growth markets that have demanding performance, design flexibility, cost and time-to-market requirements. Examples of the markets and applications in which our products are used include:

TELECOMMUNICATIONS AND DATA COMMUNICATIONS

Telecommunications and data communications companies require logic devices with high performance, low power consumption and design flexibility. QuickLogic's single-chip QuickRAM devices meet this need by providing comprehensive solutions that eliminate the need for multiple chip solutions. Alcatel uses our QuickRAM products in their fiber optic Lightwave transmission equipment.

VIDEO/AUDIO, GRAPHICS AND IMAGING

Honeywell uses our QuickRAM and FPGA products for their Primus Epic commercial avionics display systems. Their applications for QuickLogic's devices include flight data managers, back panel interfaces, flat panel display interfaces, and PCI interfaces.

INSTRUMENTATION AND TEST

Instrumentation and industrial controls manufacturers require logic devices with low power consumption, high reliability and, often, high performance. Teradyne uses our QuickRAM and FPGA devices in their semiconductor test equipment.

HIGH-PERFORMANCE COMPUTING

IBM uses our FPGA devices in numerous applications, including controllers for its redundant array of independent disks, or RAID, products. Compaq Computer also uses our FPGAs in their Alpha-based workstations and servers.

MILITARY SYSTEMS

Military electronics systems manufacturers have demanding reliability and performance requirements. Military applications require devices that remain configured even when power is lost or interrupted. Our ViaLink technology creates connections within the device which are permanent, unlike reprogrammable FPGAs, which must be reconfigured after losing power. We provide several product lines that are specially

assembled and tested to meet demanding military requirements. Hamilton Standard, a division of United Technologies, uses our FPGA devices for a flight computer in the F-117 stealth fighter.

CUSTOMERS

Through our ten years of business in the FPGA market, we have developed a strong customer base. Our customers include leading systems manufacturers, such as IBM, which recently added QuickLogic to its recommended supplier list for high performance FPGA products. The following chart provides a representative list by industry of our current customers:

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INDUSTRY	CUSTOMER	APPLICATION
<S>	<C>	<C>
Data Communications and Telecommunications	Alcatel	Fiber optic transmission equipment
	Ericsson	GSM base stations
	IBM	Data encryption, network servers
	NEC	PBX electronics, wireless base stations
	Philips	Data encryption
Video/Audio, Graphics and Imaging	Digidesign	PC-based audio editing
	Eastman Kodak	High-speed video motion analysis
	Honeywell	Aircraft navigation and flight controls

	Mitsubishi	Large screen displays
	NEC	Solid state video cameras
	Sony	Industrial video cameras
	Texas Instruments	Digital micro mirror applications
Instrumentation and Test	ABB	Industrial power management systems
	LTX	Semiconductor test equipment
	National Instruments	PC-based instrumentation boards
	Teradyne	Semiconductor test equipment
	Toshiba	Mail sorting equipment
High-Performance Computing	Compaq Computer	Alpha processor motherboards
	IBM	RAID controller, ThinkPad display controls
	Mitsubishi	Mobile PC pen-input display controllers
Military Systems	B.F. Goodrich	Launch vehicle for Delta Four rockets
	DY-4	VME-based computer systems
	Hamilton Standard	Flight computers
	Hughes Aircraft	Helicopter motor controls and radar
	McDonnell Douglas	C-17 flight controllers
	Raytheon	Tornado missile

PRODUCTS

We make field programmable gate arrays and embedded standard products based on our ViaLink technology and pASIC architecture. Each product family includes a range of devices to address differing performance and cost requirements. A variety of package types are available to satisfy varying customer requirements for physical size and the number of input and output connections to the circuit board. We also offer most of our devices in commercial, industrial and military temperature ranges.

FIELD PROGRAMMABLE GATE ARRAYS

Our pASIC products are general purpose FPGAs that address the high-performance segments of the programmable logic market. Our current product line consists of three families of FPGAs. Each of these product families include devices with a range of logic capacities and number of input and output pins. Having such a range of devices is important to design engineers whose device requirements can vary

broadly from one application to another. Smaller devices address simpler applications at lower cost, while larger devices cost more but can support larger and more complex applications. The following tables describe these families.

PASIC 3 FPGA FAMILY

DEVICE	MAXIMUM LOGIC CAPACITY (GATES)	INPUTS AND OUTPUTS(#)	INTRODUCTION DATE
QL3004	4,000	76	Q3 1999
QL3012	12,000	118	Q2 1998
QL3025	25,000	204	Q4 1997
QL3040	40,000	252	Q3 1998
QL3060	60,000	316	Q2 1998

PASIC 2 FPGA FAMILY

DEVICE	MAXIMUM LOGIC CAPACITY (GATES)	INPUTS AND OUTPUTS(#)	INTRODUCTION DATE
QL2003	6,000	118	Q1 1997
QL2005	12,000	156	Q4 1996
QL2007	18,000	174	Q4 1995

QL2009..... 25,000 225 Q2 1996
</TABLE>

PASIC 1 FPGA FAMILY

<TABLE>
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DEVICE	MAXIMUM LOGIC CAPACITY (GATES)	INPUTS AND OUTPUTS(#)	INTRODUCTION DATE
<S>	<C>	<C>	<C>
QL8x12B.....	2,000	64	Q4 1991
QL12x16B.....	4,000	88	Q4 1992
QL16x24B.....	8,000	122	Q4 1993
QL24x32B.....	16,000	180	Q2 1995

</TABLE>

EMBEDDED STANDARD PRODUCTS

ESPs are single chip solutions that combine the system-level functionality of ASSPs with the flexibility of FPGAs. ESPs link blocks of user-configurable standard functions with field programmable logic through a high-performance interface. We have introduced our first two lines of ESPs, the QuickRAM and QuickPCI families.

QUICKRAM. Our QuickRAM family of products, which began shipping in June 1998, combines blocks of high-performance, embedded memory with our high-speed programmable logic. The QuickRAM family includes five devices that span a range of logic and memory sizes, allowing design engineers to choose the optimal part for a particular application. Larger devices feature more memory and logic supporting more complex designs, while smaller devices offer lower cost. The QuickRAM family includes four available devices and one planned device that span a wide range of logic and memory sizes.

QUICKRAM ESP FAMILY

<TABLE>
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DEVICE	MEMORY CAPACITY (BITS)	MAXIMUM LOGIC CAPACITY (GATES)	INPUTS AND OUTPUTS(#)	INTRODUCTION DATE
<S>	<C>	<C>	<C>	<C>
QL4009.....	9,216	6,000	82	Q3 1999
QL4016.....	11,520	12,000	118	Q2 1999
QL4036.....	16,128	25,000	204	Q4 1998
QL4058.....	20,736	40,000	252	Q2 1999
QL4090.....	25,344	60,000	316	Q2 1998

</TABLE>

QUICKPCI. The PCI bus, or Peripheral Component Interconnect, is a standard hardware architecture that manages the transfer of data among major components in an electronic system at high speed. The master PCI bus function controls the PCI bus while the target function only operates under the control of the PCI bus. The QuickPCI family includes five devices that span a range of PCI bus capabilities and memory and programmable logic capacities, with both master and target functions. Our QuickPCI family of products combines high-performance embedded PCI bus controllers with our high-speed programmable logic. We completed development of our first QuickPCI product in April 1999, and we have shipped development quantities of devices to several customers.

The PCI bus is available in two basic configurations: 32 bits wide and 64 bits wide. Clock speeds for the PCI bus range from 33MHz to 75MHz. Devices which support the smaller, slower PCI configurations cost less than devices which support the wider, faster configurations. While many semiconductor vendors offer devices that address one particular PCI configuration, very few offer a full range of devices to meet all of the possible configurations.

QUICKPCI ESP FAMILY

<TABLE>
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DEVICE	PCI BUS FUNCTION	MAX. PCI BUS SPEED/WIDTH	MEMORY CAPACITY (BITS)	LOGIC CAPACITY (GATES)	INTRODUCTION DATE

QL5030.....	Target	33MHz/32-bits	11,500	4,500	Q3 1999
QL5130.....	Target	33MHz/32-bits	16,000	17,500	Q4 1999
QL5032.....	Master/Target	33MHz/32-bits	16,000	14,500	Q2 1999
QL5232.....	Master/Target	33MHz/32-bits	25,344	49,500	Q3 1999
QL5064.....	Master/Target	75MHz/64-bits	25,344	30,000	Q3 1999

QUICKDSP. Digital Signal Processing, or DSP, is the use of mathematical functions to modify digital signals in desirable ways. For example, using DSP techniques, engineers can design systems for such diverse purposes as eliminating echoes from telephone conversations, increasing data transmission rates for Internet access, or reducing the file size of electronic medical images.

The QuickDSP family combines a set of Embedded Computational Units, or ECUs, with high-performance programmable logic and memory. These ECUs have been optimized to implement the mathematical operations inherent in DSP applications with high speed and efficiency. The QuickDSP family includes four devices, each with differing amounts of ECUs, programmable logic, and memory-allowing design engineers to choose the optimal device for their application.

QUICKDSP ESP FAMILY

DEVICE	ECU BLOCKS(#)	MAXIMUM MEMORY CAPACITY (BITS)	LOGIC CAPACITY (GATES)	INPUTS AND OUTPUTS(#)	INTRODUCTION DATE
QL7100.....	10	46,100	292,000	256	Expected Q3 2000
QL7120.....	12	55,300	373,000	320	Expected Q3 2000
QL7160.....	16	73,700	558,000	448	Expected Q2 2000
QL7180.....	18	82,900	662,000	512	Expected Q2 2000

FPGA AND ESP DEVELOPMENT TOOLS

Our FPGA and ESP devices are supported by a complete range of development tools including software and device programming hardware.

QUICKWORKS. QuickWorks is a fully integrated design solution consisting of internally developed and licensed third-party software operating on Microsoft Windows. QuickWorks includes industry-standard, hardware description languages, including VHDL and Verilog, as well as schematic and mixed-mode entry for fast and efficient logic design. Our suite provides a complete FPGA software solution, including design entry, logic synthesis, place and route, and simulation. A derivative product, called QuickWorks-Lite, offers basic design entry via schematic capture along with place and route free to designers.

QUICKTOOLS. QuickTools provides optimization, place and route, timing analysis and back-annotation support for all our devices on UNIX platforms. The QuickTools package provides a software solution for designers who use Cadence, Mentor, Synario Design Automation, Synopsys, Veribest, Viewlogic Systems or other third-party software tools for design entry, synthesis or simulation.

PROGRAMMING HARDWARE. After a design has been completed using our software, the device is configured using our line of DeskFAB programming hardware and associated device adapters.

SALES, MARKETING AND TECHNICAL SUPPORT

We sell our products through a network of sales managers, independent sales representatives and electronics distributors in North America, Europe and Asia. In addition to our corporate headquarters in Sunnyvale, we have regional sales operations in Los Angeles, Dallas, Boston, Raleigh, Chicago, London, Tokyo, Munich, Shanghai and Hong Kong. Our direct sales organization consists of a staff of 24, including sales managers, field application engineers and administrative personnel. In North America, our six sales managers direct the activities of 19 independent sales representative firms operating out of more than 40 offices totaling approximately 180 sales representatives, as well as the activities of four electronics distributors with more than 230 locations. Internationally, three sales managers direct the activities of nine distributors

and two independent sales representatives in Europe and nine distributors in Asia. Our marketing organization consists of 17 employees. All of the foregoing numbers are as of February 29, 2000.

Four major distributors, Arrow Electronics, Bell Microproducts, Future Electronics and Sterling Electronics accounted for approximately 51% of our sales in 1999. Our international sales were 43%, 47% and 48% of our total sales for 1997, 1998 and 1999, respectively. Although we have contracts with our distributors, any of them may terminate their relationship with us on short notice. The loss of one or more of our principal distributors, or our inability to attract new distributors, would materially harm our business. We may lose distributors in the future and we may be unable to recruit additional or replacement distributors. As a result, our future performance will depend in part on our ability to retain our existing distributors and attract new distributors that will be able to market, sell and support our products effectively. We anticipate that sales to customers located outside the United States will continue to represent a significant portion of our total sales in future periods and the trend of foreign customers

accounting for an increasing portion of our total sales may continue. We believe that no end customer accounted for more than 5% of sales in 1999.

We sell our products on a purchase order basis through our distributors and direct sales channels, and our distributors or customers may cancel purchase orders at any time with little or no penalty. In addition, our distributor agreements generally permit our distributors to return unprogrammed products to us. Contractually, our distributors are permitted to return up to 10%, by value, of the products they purchase from us every six months.

We provide systems manufacturers with comprehensive technical support, which we believe is critical to remaining competitive in the markets we serve. As of February 29, 2000, our applications support organization included four direct field application engineers and over 200 application engineers employed by our distributors. These application engineers provide pre-sales and on-site technical support to customers. Application support is also provided by six factory-based customer engineers who offer the majority of post-sale support through a dedicated customer support hotline. In 1998, we established a design center to develop new embedded functions for ESPs, and to provide in-depth, system-level technical support to our customers.

Our WebASIC program allows systems manufacturers to download our design software from our web site and create a custom design for a QuickLogic device at their desktop. They can then transmit the design data to us via e-mail and request configured sample devices. We also use our web site to provide product documentation and technical support information.

RESEARCH AND DEVELOPMENT

Our future success will depend to a large extent on our ability to rapidly develop and introduce new products and enhancements to our existing products that meet emerging industry standards and satisfy changing customer requirements. We have made and expect to continue to make substantial investments in research and development and to participate in the development of new and existing industry standards.

As of February 29, 2000, the research and development staff consisted of 42 employees. Our research and development efforts are focused on standard function development and integration, device architecture, development tools and foundry process development. Our standard function development and integration personnel create circuit designs for inclusion in our ESP products. They also evaluate circuit designs by third parties for inclusion in our ESP products and integrate those circuit designs with our FPGA technology. Our device architecture personnel develop new and improved architectures for our FPGA and ESP products to better serve the needs of our customers. Our software engineering group develops place and route tools, which fit the design into specific logic cell elements within a device and determine the necessary interconnections. They also develop delay modeling tools, which estimate the timing of all the circuit paths for accurate simulation. The software group incorporates third-party software tools into the QuickWorks design software suite, and develops the design libraries needed for the QuickWorks and QuickTools products to integrate with third-party design environments. Our process engineering group maintains our proprietary wafer manufacturing processes, oversees product manufacturing and process development with our third-party foundries, and is involved in ongoing process improvements to increase yields and optimize device characteristics.

Our research and development expense for 1997, 1998 and 1999 were $6.2 million, $6.3 million and $7.4 million, respectively. We anticipate that we will continue to commit substantial resources to research and development in the future.

MANUFACTURING

We have established close relationships with third-party manufacturers for our wafer fabrication, package assembly, test and programming requirements to ensure stability in the supply of our products and minimize the risk of localized capacity constraints.

We outsource all of our wafer manufacturing to Taiwan Semiconductor Manufacturing Company at its Taiwan facilities and Cypress Semiconductor Corporation at its Round Rock, Texas facility. TSMC manufactures our pASIC 3, QuickRAM and QuickPCI product families using a four-layer metal, 0.35 micron CMOS process on eight-inch wafers. Cypress manufactures our pASIC 1 and pASIC 2 product families using a three-layer metal, 0.65 micron CMOS process on six-inch wafers. Our foundry agreement with TSMC is effective through August 2002 with successive automatic one-year renewal terms. We have committed to purchase approximately $9.4 million under this agreement in 2000. We recently amended our foundry agreement with Cypress to extend the term through 2005. Each of our foundry agreements guarantee capacity availability and provide for volume commitments. We purchase all of our pASIC 1 and pASIC 2 requirements from Cypress. TSMC's manufacturing commitment is based upon our forecasted requirements. TSMC requires that we purchase a minimum percentage of our total production requirements in any one year from them.

We outsource our product packaging, test and programming to Amkor and ChipPAC at their South Korea facilities and to Advanced Semiconductor Engineering at its Taiwan facility.

COMPETITION

The semiconductor industry is intensely competitive and is characterized by constant technological change, rapid rates of product obsolescence and price erosion. Our existing competitors include suppliers of conventional standard products, such as PLX Technology and Applied Micro Circuits Corporation, or AMCC; suppliers of complex programmable logic devices, or CPLDs, including Lattice Semiconductor and Altera; and suppliers of FPGAs, particularly Xilinx and Actel. The PLD market is dominated by Xilinx and Altera, which together control over 60% of the market, according to inSearch Research, a semiconductor market research firm. Xilinx dominates the FPGA segment of the market while Altera dominates the CPLD segment of the market. We also face competition from companies that offer standard gate arrays, which can be obtained at a lower cost for high volumes and may have gate densities and performance equal or superior to our products. As we introduce additional ESPs, we will also face competition from standard product manufacturers who are already servicing or who may decide to enter the markets addressed by these new ESP devices. In addition, we expect significant competition in the future from major domestic and international semiconductor suppliers. We also may face competition from suppliers of products based on new or emerging technologies.

We believe that important competitive factors in our market are length of development cycle, price, performance, installed base of development systems, adaptability of products to specific applications, ease of use and functionality of development system software, reliability, technical service and support, wafer fabrication capacity and sources of raw materials, and protection of products by effective utilization of intellectual property laws.

TECHNOLOGY

We believe that our FPGA and ESP products have distinct advantages over traditional FPGA solutions and multiple chip solutions combining FPGAs and ASSPs with regard to speed, design flexibility, cost and time-to-market. Our key technologies are the ViaLink programmable metal technology, pASIC architectures, and the QuickWorks and QuickTools design software.

VIALINK PROGRAMMABLE METAL TECHNOLOGY. Our ViaLink programmable metal technology embeds programmable switches between the metal layers of a device without consuming silicon surface area. As a

result, we are able to provide a programmable switch at every intersection in the wire grid. The abundance of programmable switches allows for more complex

paths between logic cells and facilitates full utilization of an FPGA's logic cells and input/output pins. As a consequence, system designers using QuickLogic FPGAs can be assured that their design can consume all of the logic capacity of the FPGA and will have enough resources to route their signals in very complex designs. Changes in our customers' designs will not move the positions of their inputs and outputs. The programming resources of our FPGAs allow designers to select smaller, less expensive QuickLogic FPGAs to implement their designs as opposed to customary SRAM-based FPGAs. In addition, our ViaLink technology also features lower resistance and capacitance than competing programming technologies, thereby optimizing the device's performance.

PASIC ARCHITECTURE. Our FPGA device architecture consists of logic cells, routing wires and interconnect switches. Our pASIC logic cell is optimized to efficiently implement a wide range of logic functions at high speed. Each cell can implement one large function, five smaller independent functions, or any combination in-between. The logic cell has abundant inputs that allow many user functions to be implemented with a single logic delay, resulting in high performance. The flexibility of the pASIC architecture is especially important for designs synthesized from hardware design languages. The pASIC architecture gives logic synthesis tools the needed degrees of freedom for high logic utilization without sacrificing performance.

QUICKWORKS AND QUICKTOOLS DESIGN SOFTWARE. Our comprehensive QuickWorks design software provides high-level design entry, schematic capture, logic synthesis, functional and timing simulation, placement and routing on the Windows operating system. QuickWorks incorporates standard design languages, Verilog and VHDL, and leading third-party software to integrate with all leading third-party design environments to support our pASIC products. A derivative product, called QuickWorks-Lite, offers basic design entry via schematic capture along with place and route free to designers. QuickTools is QuickLogic's place and route software for UNIX platforms. These tools optimize designs for device utilization and in-system operation speed and create an output file which allows users to transfer their designs to our programmable devices.

EMPLOYEES

As of February 29, 2000, we had a total of 155 employees worldwide, with 43 people in operations, 42 people in research and development, 25 people in sales, 17 people in marketing, 24 people in administration and four people in management information systems. We believe that our future success will depend in part on our continued ability to attract, hire and retain qualified personnel. None of our employees is represented by a labor union, and we believe our employee relations are good.

INTELLECTUAL PROPERTY

Our future success and competitive position depend upon our ability to obtain and maintain the proprietary technology used in our principal products. We hold 67 U.S. patents and have 22 pending applications for additional U.S. patents containing claims covering various aspects of programmable integrated circuits, programmable interconnect structures and programmable metal devices. In addition, we have three patent applications pending in Japan. Our issued patents expire between 2009 and 2018. We have also registered six of our trademarks in the U.S. with applications to register an additional two trademarks now pending.

Because it is critical to our success that we are able to prevent competitors from copying our innovations, we intend to continue to seek patent protection for our products. The process of seeking patent protection can be long and expensive, and we cannot be certain that any currently pending or future applications will actually result in issued patents, or that, even if patents are issued, they will be of sufficient scope or strength to provide meaningful protection or any commercial advantage to us.

Furthermore, others may develop technologies that are similar or superior to our technology or design around the patents we own.

We also rely on trade secret protection for our technology, in part through confidentiality agreements with our employees, consultants and third parties. However, employees may breach these agreements, and we may not have adequate remedies for any breach. In any case, others may come to know about or determine our trade secrets through a variety of methods. In addition, the laws of certain territories in which we develop, manufacture or sell our products may not protect our intellectual property rights to the same extent as do the laws of the United States.

In March 1997, we entered into a patent cross-license agreement with Cypress, whereby we granted Cypress a nonexclusive license to our patents and intellectual property rights in exchange for Cypress' nonexclusive license to their programmable logic technology patents. In August 1998, we also entered into a patent cross-license agreement with Actel pursuant to which we have each granted the other a nonexclusive license to certain of our respective programmable logic device technology patents. We anticipate that we will continue to enter into licensing arrangements in the future; however, it is possible that desirable licenses will not be available to us on commercially reasonable terms. If we lose existing licenses to key technology, or are unable to enter into new licenses which we deem important, it could materially harm our business.

From time to time, we receive letters alleging patent infringement or inviting us to take a license to other parties' patents. We evaluate these letters on a case-by-case basis. In September 1999, we received an offer to license a patent related to field programmable gate array architecture. It is too early for us to determine whether this license would be necessary or useful and obtainable at a reasonable price. Offers such as these may lead to litigation if we reject the opportunity to obtain the license.

We have entered into technology license agreements with third parties which give those parties the right to use patents and other technology developed by us, and which give us the right to use patents and other technology developed by them. The failure to obtain a license from a third party for technology used by us could cause us to incur substantial liabilities and to suspend the manufacture or shipment of products or our use of processes requiring the technology. Litigation could result in significant expenses to us, adversely affect sales of the challenged product or technology and divert the efforts of our technical and management personnel, whether or not the litigation is determined in our favor. In the event of an adverse result in any litigation, we could be required to pay substantial damages, cease the manufacture, use, sale or importation of infringing products, expend significant resources to develop or acquire non-infringing technology, and discontinue the use of processes requiring the infringing technology or obtain licenses to the infringing technology. We may not be successful in the development or acquisition, or the necessary licenses may not be available under reasonable terms, and any development, acquisition or license could require expenditures by us of substantial time and other resources. Any of these developments would have a material adverse effect on our business. We may be unable to adequately protect our intellectual property rights, and may face significant expenses as a result of future litigation.

EXECUTIVE OFFICERS AND DIRECTORS

The following table sets forth certain information concerning our current executive officers and directors as of March 15, 2000:

<TABLE>
<CAPTION>

NAME	AGE	POSITION
<S>	<C>	<C>
E. Thomas Hart	58	President, Chief Executive Officer and Director
John M. Birkner	56	Vice President, Chief Technical Officer
Michael R. Brown	50	Vice President, Worldwide Sales
Andrew K. Chan	49	Vice President, Research and Development
Hua-Thye Chua	64	Vice President, Process Technology and Director
Reynold W Simpson	51	Vice President, Operations
Bill J. Smithson	57	Vice President, Engineering
Arthur O. Whipple	52	Vice President, Finance, Chief Financial Officer and Secretary
Ronald D. Zimmerman	51	Vice President, Human Resources
Irwin Federman	64	Chairman of the Board of Directors

Donald P. Beadle..... 64 Director

Michael J. Callahan..... 64 Director
</TABLE>

E. THOMAS HART has served as our President, Chief Executive Officer and a member of our board of directors since June 1994. Prior to joining QuickLogic, Mr. Hart was Vice President and General Manager of the Advanced Networks Division at National Semiconductor, a semiconductor manufacturing company, where he worked from September 1992 to June 1994. Prior to joining National Semiconductor Corporation, Mr. Hart was a private consultant from February 1986 to September 1992 with Hart Weston International, a technology-based management consulting firm. Mr. Hart holds a B.S.E.E. from the University of Washington.

JOHN M. BIRKNER, a co-founder of QuickLogic, has served with us since April 1988, serving as Vice President, Chief Technical Officer since 1993. From September 1975 to June 1986, Mr. Birkner was a fellow at Monolithic Memories, a semiconductor manufacturing company. Mr. Birkner holds a B.S.E.E. from the University of California, Berkeley and an M.S.E.E. from the University of Akron.

MICHAEL R. BROWN has served as our Vice President, Worldwide Sales since January 1999. From 1984 until January 1999, he was employed by Hitachi America, a semiconductor manufacturing company, in a variety of sales management positions, most recently as the Vice President of Sales for the Americas. Mr. Brown holds a B.A. in Kinesiology/Psychology from California State University, Northridge and attended the U.S. Navy Aviation Electronics School. Mr. Brown holds a certificate in Advanced Management from Stanford University.

ANDREW K. CHAN, a co-founder of QuickLogic, has served with us since April 1988, most recently as Vice President, Research and Development. Prior to joining QuickLogic, Mr. Chan was a design engineering manager at Monolithic Memories. Mr. Chan holds a B.S.E.E. in Electrical Engineering from Washington State University and an M.S.E.C. in Electrical Sciences from the University of New York, Stonybrook.

HUA-THYE CHUA, a co-founder of QuickLogic, has served as a member of our board of directors since QuickLogic's inception in April 1988. Since December 1996, Mr. Chua has served as our Vice President, Process Technology. He served as our Vice President of Technology Development from April 1989 to December 1996. During the prior 25 years, Mr. Chua worked at semiconductor manufacturing companies,

including Fairchild Semiconductor, Intel and Monolithic Memories. Mr. Chua holds a B.S.E.E. from Ohio University and an M.S.E.E. from the University of California, Berkeley.

REYNOLD W. SIMPSON has served as our Vice President, Operations since August 1997. From February 1996 to July 1997, Mr. Simpson was Vice President of Manufacturing at GateField, a semiconductor manufacturing company. Prior to joining GateField, Mr. Simpson was Operations Manager at LSI Logic, a semiconductor manufacturing company, from March 1990 to February 1996 and Quality Director from February 1989 to March 1990. Mr. Simpson holds a Mechanical Engineering Certificate from the Coatbridge Polytechnic Institute in Scotland, a degree in Technical Horology (Mechanical Engineering) from the Barmulloch Polytechnic Institute in Scotland and studied for a degree in Electronic Engineering at the Kingsway Polytechnic Institute in Scotland.

BILL J. SMITHSON has served as our Vice President, Engineering since September 1999. From April 1991 to September 1999, Mr. Smithson was Vice President, Semiconductor Technology at Adaptec Inc., a developer and manufacturer of input/output technology products. From 1987 to 1990, Mr. Smithson was Division Director, Integrated Circuit Research and Development at Data General Corporation, a semiconductor corporation. Mr. Smithson has also held senior management positions at other semiconductor companies, including VLSI Technology, Inc., National Semiconductor Corporation, and Motorola, Inc. Mr. Smithson holds a B.S.E.E. from the University of Missouri at Rolla, an M.S.E.E. from Arizona State University and an M.B.A. from Santa Clara University.

ARTHUR O. WHIPPLE has served as our Vice President, Finance, Chief Financial Officer and Secretary since April 1998. From April 1994 to April 1998, Mr. Whipple was employed by ILC Technology, a manufacturer of high performance lighting products, as its Vice President of Engineering and by its subsidiary, Precision Lamp, a manufacturer of high-performance lighting products, as its Vice President of Finance and Operations. From February 1990 to April 1994,

Mr. Whipple served as the President of Aqua Design, a privately-held provider of water treatment services and equipment. Mr. Whipple holds a B.S.E.E. from the University of Washington and an M.B.A. from Santa Clara University.

In May 1990, Mr. Whipple reached a settlement with the SEC in connection with an action brought by the SEC concerning the accounting treatment for certain revenue reflected in the financial statements of URS Corporation, then known as Thortec, in 1986 and 1987. Mr. Whipple was Vice President and Treasurer at URS Corporation during that period. Mr. Whipple consented to the entry of an injunction with the SEC without admitting or denying any of the SEC's allegations, and there was no adjudication or findings of fact. The injunction bars Mr. Whipple from aiding and abetting the filing of any report with the SEC that contains an untrue statement of material fact and aiding and abetting the failure to keep accurate and fair books and records. Our Audit Committee conducted a detailed investigation into Mr. Whipple's involvement in the matter, and concluded that nothing concerning that matter affects Mr. Whipple's integrity or ability to serve as our Chief Financial Officer.

RONALD D. ZIMMERMAN has served as our Vice President, Human Resources since October 1996. From August 1988 to October 1996, Mr. Zimmerman was Human Resources Director of the Analog Products Group at National Semiconductor Corporation, as well as group human resources director of the corporate technology and quality/reliability organizations and the human resources director of corporate administration. Mr. Zimmerman holds a B.A. in Sociology and Psychology and an M.A. in Psychology from San Jose State University.

IRWIN FEDERMAN has served as chairman of our board of directors since September 1989. Mr. Federman has been a general partner of U.S. Venture Partners, a venture capital company, since 1990. From 1988 to 1990, he was a Managing Director of Dillon Read & Co., an investment banking firm, and a general partner in its venture capital affiliate, Concord Partners. Mr. Federman serves on the boards of directors of the following public companies: TelCom Semiconductor, a semiconductor company; SanDisk, a semiconductor company; Western Digital, a disk drive manufacturer; Komag, a thin film media manufacturer; NeoMagic, a developer of multimedia accelerators; and Check Point Software Technologies, a network

security software company. Mr. Federman holds a B.S. in Economics from Brooklyn College, is a Certified Public Accountant, and holds an honorary Doctorate of Engineering Science from Santa Clara University.

DONALD P. BEADLE has served as a member of our board of directors since July 1997. Since June 1994, Mr. Beadle has been President of Beadle Associates, a consulting firm. From May 1997 to July 1997, Mr. Beadle was a consultant at Interwave Communications, a developer of microcell systems, where he served as Acting Vice President of Sales and Sales Operations. From October 1994 to December 1996, he was a consultant for Asian business development at National Semiconductor. At National Semiconductor, he was Managing Director, Southeast Asia from 1993 until June 1994, Vice President of Worldwide Marketing and Sales, International Business Group from 1987 until 1993, and Managing Director, Europe from 1982 to 1986. Mr. Beadle was employed by National Semiconductor in executive sales and marketing positions for 34 years until June 1994, at which time he was Executive Vice President, Worldwide Sales and Marketing. Mr. Beadle serves on the board of directors of one public company, HMT Technology, a disk media manufacturer. He received his technical education at the University of Connecticut and the Bridgeport Institute of Engineering.

MICHAEL J. CALLAHAN has served as a member of our board of directors since July 1997. Since March 1990, Mr. Callahan has served as Chairman of the Board, President and Chief Executive Officer of Waferscale Integration, a producer of peripheral integrated circuits. From 1987 to March 1990, Mr. Callahan was President of Monolithic Memories, or MMI, which became a subsidiary of Advanced Micro Devices, a semiconductor manufacturing company, or AMD. Also during this time, he was Senior Vice President of Programmable Products at AMD. From 1978 to 1987, Mr. Callahan held a number of positions at MMI including Vice President of Operations and Chief Operating Officer. Prior to joining MMI, he worked at Motorola Semiconductor, a semiconductor manufacturing company, for 16 years where he was Director of Research and Development as well as Director of Linear Operations. Mr. Callahan holds a B.S.E.E. from the Massachusetts Institute of Technology.

EXECUTIVE OFFICERS

Our executive officers are elected by, and serve at the discretion of, our board of directors. There are no family relationships among our directors and

officers.

BOARD OF DIRECTORS

We currently have authorized five directors. Our directors consist of Messrs. Beadle, Callahan, Chua, Federman and Hart. All directors hold office until the next annual meeting of stockholders or until their successors are duly qualified and elected. Our certificate of incorporation provides that, as of the first annual meeting of stockholders following our initial public offering, our board of directors will be divided into three classes, each with staggered three-year terms. As a result, only one class of directors will be elected at each annual meeting of our stockholders, with the other classes continuing for the remainder of their respective three-year terms. Messrs. Beadle and Callahan have been designated as Class I directors, whose term expires at the 2000 annual meeting of stockholders; Messrs. Chua and Federman have been designated as Class II directors, whose term expires at the 2001 annual meeting of stockholders; and Mr. Hart has been designated as a Class III director, whose term expires at the 2002 annual meeting of stockholders.

BOARD COMMITTEES

Our board of directors has an audit committee and a compensation committee.

AUDIT COMMITTEE. The audit committee was formed in June 1995 and currently consists of Messrs. Beadle, Callahan and Federman. The audit committee reviews the results and scope of the annual audit and other services provided by our independent accountants, reviews and evaluates our internal control functions and monitors financial transactions between us and our employees, officers and directors.

COMPENSATION COMMITTEE. The compensation committee was formed in June 1995 and currently consists of Messrs. Beadle, Callahan and Federman. The compensation committee administers the 1989 stock option plan, 1999 stock plan and 1999 employee stock purchase plan, and reviews the compensation and benefits for our executive officers.

COMPENSATION COMMITTEE INTERLOCKS AND INSIDER PARTICIPATION

Prior to establishing the compensation committee, the board of directors as a whole performed the functions delegated to the compensation committee. No member of the compensation committee or executive officer of QuickLogic has a relationship that would constitute an interlocking relationship with executive officers or directors of another entity.

ITEM 2. PROPERTIES

Our principal administrative, sales, marketing, research and development and final testing facility is located in a building of approximately 42,624 square feet in Sunnyvale, California. This facility is leased through 2003 with an option to renew through 2006. In addition, we lease sales offices near London and in Hong Kong and an engineering office in Hillsborough, Oregon. The London office is leased through September 2004, and the Hong Kong office is leased on a month-to-month basis. The Hillsborough office is leased through December 31, 2000. We believe that our existing facilities are adequate for our current needs.

ITEM 3. LEGAL PROCEEDINGS

We have no pending or threatened litigation.

In September 1999, we received an offer to license a patent related to field programmable gate array architecture. It is too early for us to determine whether this license would be necessary or useful, or whether a license would be obtainable at a reasonable price. Offers such as this may lead to litigation if we reject the opportunity to obtain the license. We believe that the resolution of this matter will not have a material adverse effect on our financial condition or results of operations.

The semiconductor industry has experienced a substantial amount of litigation regarding patent and other intellectual property rights. From time to time, we have has received and may receive in the future, communications alleging that our products or our processes may infringe on product or process technology rights held by others. We may in the future be involved in litigation with respect to alleged infringement by us of another party's patents. In the future, we may be involved with litigation to:

- Enforce our patents or other intellectual property rights.

- Protect our trade secrets and know-how.

- Determine the validity or scope of the proprietary rights of others.

- Defend against claims of infringement or invalidity.

- Such litigation has in the past and could in the future result in substantial costs and diversion of management resources. Such litigation could also result in payment of substantial damages and/or royalties or prohibitions against utilization of essential technologies, and could have a material adverse effect on our business, financial condition and results of operations.

We settled our patent litigation with Actel Corporation in August 1998. We paid our remaining obligation of $5,750,000 on November 3, 1999.

ITEM 4. SUBMISSION OF MATTERS TO A VOTE OF SECURITY HOLDERS

No matters were submitted to a vote of security holders during the fourth quarter of the fiscal year covered by this report.

PART II

ITEM 5. MARKET FOR THE REGISTRANT'S COMMON EQUITY AND RELATED STOCKHOLDER MATTERS

Our Common Stock has been traded on The Nasdaq Stock Market's National Market under the symbol "QUIK" since October 15, 1999, the date of our initial public offering. The following table sets forth for the periods indicated the high and low closing prices for the Common Stock, as reported on The Nasdaq Stock Market's National Market:

<TABLE>
<CAPTION>

	HIGH	LOW
<S>	<C>	<C>
FISCAL YEAR ENDING DECEMBER 31, 1999		
Fourth Quarter (from October 15, 1999).....	$19.563	$12.938
FISCAL YEAR ENDING DECEMBER 31, 2000		
First Quarter (through March 27, 2000).....	$39.500	$13.750

</TABLE>

The last reported sale price of our Common Stock on The Nasdaq Stock Market's National Market was $37.688 per share on March 27, 2000. As of March 27, 2000, there were 18,160,330 shares of Common Stock outstanding that were held of record by approximately 210 stockholders.

We commenced our initial public offering on October 15, 1999 pursuant to a Registration Statement on Form S-1 (File No. 333-28833) which was declared effective by the Securities and Exchange Commission on October 14, 1999. The Company sold an aggregate of 3,770,635 shares of Common Stock in our initial public offering at an initial price to the public of $10.00 per share. In addition, a selling stockholder sold 3,896,415 shares of Common Stock in our initial public offering at an initial price to the public of $10.00 per share. Our initial public offering has terminated and all shares have been sold. The managing underwriters of our initial public offering were Robertson Stephens, Bear, Stearns & Co. Inc. and SoundView Technology Group. Aggregate proceeds from our initial public offering were $76,670,500, which includes $10,000,500 in aggregate proceeds due to the exercise of the underwriters' option to purchase shares to cover over-allotments.

We paid underwriters' discounts and commissions of $2,639,444.50 and no additional offering expenses in connection with our initial public offering. The total expenses we paid in our initial public offering were $1,190,000, and the net proceeds to us of our initial public offering were $33.9 million.

From October 14, 1999, the effective date of the Registration Statement, to December 31, 1999, the ending date of the reporting period, the approximate amount of net offering proceeds used were $6.0 million for general business operations. See "Management's Discussion and Analysis of Financial Condition and Results of Operations."

DIVIDEND POLICY

We have never declared or paid any dividends on our capital stock. We currently expect to retain future earnings, if any, for use in the operation and expansion of our business and do not anticipate paying any cash dividends in the foreseeable future.

ITEM 6. SELECTED FINANCIAL DATA

<TABLE>
<CAPTION>

	YEAR ENDED DECEMBER 31,				
	1995	1996	1997	1998	1999
	(IN THOUSANDS, EXCEPT PER SHARE DATA)				
<S>	<C>	<C>	<C>	<C>	<C>
STATEMENT OF OPERATIONS DATA:					
Revenue	$15,148	$23,758	$ 28,460	$30,007	$39,785
Cost of revenue	7,739	11,158	16,855	14,303	17,103
Gross profit	7,409	12,600	11,605	15,704	22,682
Operating expenses:					
Research and development	3,599	4,642	6,235	6,294	7,355
Selling, general and administrative	5,770	7,730	10,981	9,368	12,618
Contract termination and legal(1)	2,700	4,125	28,309	--	--
Net operating income (loss)	(4,660)	(3,897)	(33,920)	42	2,709
Interest expense	(200)	(60)	(162)	(161)	(97)
Interest income and other, net	153	360	434	364	549
Net income (loss)	$(4,707)	$(3,597)	$(33,648)	$ 245	3,161
Net income (loss) per share:					
Basic	$ (7.59)	$ (4.66)	$ (10.41)	$ 0.06	$ 0.42
Diluted	$ (7.59)	$ (4.66)	$ (10.41)	$ 0.02	$ 0.19
Weighted average shares:					
Basic	620	772	3,232	4,231	7,615
Diluted	620	772	3,232	14,645	16,400

</TABLE>

<TABLE>
<CAPTION>

	DECEMBER 31,				
	1995	1996	1997	1998	1999
	(IN THOUSANDS)				
<S>	<C>	<C>	<C>	<C>	<C>
BALANCE SHEET DATA:					
Cash	$ 3,856	$10,336	$ 7,331	$ 7,595	$34,558
Working capital (deficit)	7,068	10,650	2,395	(3,319)	32,568
Total assets	12,199	22,577	19,951	16,168	50,482
Long-term obligations(2)	137	602	7,724	591	128
Total stockholders' equity (deficit)	7,149	11,799	(1,756)	(975)	37,005

</TABLE>

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(1) Contract termination and legal expenses include a charge of $23.0 million in the year ended December 31, 1997 for termination of an agreement with Cypress Semiconductor Corporation, and charges of $2.7 million, $4.1 million and $5.3 million in the years ended December 31, 1995, 1996 and 1997, respectively, for the legal and settlement costs associated with the Actel Corporation litigation. See notes 8 and 12 of notes to consolidated financial statements and "Management's Discussion and Analysis of Financial Condition and Results of Operations."

(2) Long term obligations at December 31, 1997 include obligations under the Actel litigation settlement. At December 31, 1998, this obligation is classified as a current liability. We paid all of our remaining obligations under the settlement on November 3, 1999. See notes 5 and 12 of notes to

consolidated financial statements.

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

THIS SECTION AND OTHER PARTS OF THIS REPORT, CONTAIN FORWARD-LOOKING STATEMENTS THAT INVOLVE RISKS AND UNCERTAINTIES. OUR ACTUAL RESULTS COULD DIFFER MATERIALLY FROM THOSE ANTICIPATED IN FORWARD-LOOKING STATEMENTS FOR MANY REASONS, INCLUDING THE RISKS DESCRIBED IN THE SECTION TITLED "RISK FACTORS" BEGINNING ON PAGE 27. YOU SHOULD READ THE FOLLOWING DISCUSSION WITH THE "SELECTED FINANCIAL DATA" AND OUR FINANCIAL STATEMENTS AND RELATED NOTES INCLUDED ELSEWHERE IN THIS REPORT.

OVERVIEW

We design and sell field programmable gate arrays, embedded standard products and associated software and programming hardware. From our inception in April 1988 through the third quarter of 1991, we were primarily engaged in product development. In 1991, we introduced our first line of field programmable gate array products, or FPGAs, based upon our ViaLink technology. FPGAs have accounted for substantially all of our product revenue to date. We currently have three FPGA product families: pASIC 1, introduced in 1991; pASIC 2, introduced in 1996; and pASIC 3, introduced in 1997. The newer product families generally contain greater logic capacity, but do not necessarily replace sales of older generation products. In fact, in 1999, pASIC 1 revenue accounted for approximately half of our total revenue.

In September 1998, we introduced QuickRAM, our first line of embedded standard products, or ESPs. Our ESPs are based on our FPGA technology. In April 1999, we introduced QuickPCI, our second line of ESPs. Revenue for our QuickRAM and QuickPCI products together accounted for approximately 6% of our total revenue in 1999. We also license our QuickWorks and QuickTools design software and sell our programming hardware, which together have typically accounted for less than 5% of total revenue.

We sell our products through three channels. First, we sell the majority of our products through distributors who have contractual rights to earn a negotiated margin on the sale of our products and who have limited rights to return unsold, unprogrammed products. We refer to these distributors as point-of-sale distributors. We defer recognition of revenue for sales to these point-of-sale distributors until after they have sold our products to systems manufacturers. As many as half of our products are programmed by us and are not returnable by these point-of-sale distributors. We recognize revenue on these products at the time of shipment. Second, we sell our products through certain foreign distributors who have no contractual rights to earn a negotiated margin and who may only return defective products to us. We recognize revenue from sales to these distributors at the time of shipment. Finally, we sell our products directly to systems manufacturers and recognize revenue at the time of shipment to these systems manufacturers. The percentage of sales derived through each of these three channels in 1998 was 54%, 32% and 14%, respectively, and 59%, 21% and 20% in 1999, respectively. During the fourth quarter of 1999, we completed the transition of our remaining foreign distributors to point-of-sale distributors.

Four distributors accounted for 27%, 10%, 10% and 6% of sales, respectively, in 1998 and the same four distributors accounted for approximately 24%, 11%, 10% and 6% of sales, respectively, in 1999. We believe that no other distributor or direct customer accounted for more than 5% of sales in 1998 or 1999. We expect that a limited number of distributors will continue to account for a significant portion of our total sales.

Our international sales were 43%, 47% and 48% of our total sales for 1997, 1998 and 1999, respectively. We expect that revenue derived from sales to international customers will continue to represent a significant and growing portion of our total revenue. All of our sales are denominated in U.S. dollars.

Average selling prices for our products typically decline rapidly during the first six to 12 months after their introduction, then decline less rapidly as the products mature. We attempt to maintain gross margins

even as average selling prices decline through the introduction of new products with higher margins and through manufacturing efficiencies and cost reductions. However, the markets in which we operate are highly competitive, and there can be no assurance that we will be able to successfully maintain gross margins. Any

significant decline in our gross margins will materially harm our business.

We outsource the wafer manufacturing, assembly and test of all of our products. We rely upon TSMC and Cypress to manufacture our products, and we rely primarily upon Amkor and ChipPAC to assemble and test our products. Under our arrangements with these manufacturers, we are obligated to provide forecasts and enter into binding obligations for anticipated purchases. This limits our ability to react to fluctuations in demand for our products, which could lead to excesses or shortages of wafers for a particular product.

We entered into an agreement with Cypress in 1992 to obtain guaranteed fabrication capacity and to secure a second source for our FPGA products. By 1997, wafer fabrication capacity was no longer scarce and we had established a customer base and reputation. In March 1997, our agreement with Cypress was terminated. In exchange for the termination and the reversion to us of the rights to the intellectual property covered by that agreement, we paid Cypress $4.5 million in cash and agreed to issue to Cypress 3,037,786 shares of our common stock, resulting in a charge of approximately $23.0 million in the first quarter of 1997.

In 1997, we recorded an accrual for legal and settlement fees of $5.3 million, associated with the settlement of patent litigation with Actel Corporation in 1998. We have made quarterly payments to Actel since the settlement date. We paid our remaining obligation under the settlement on November 3, 1999.

RESULTS OF OPERATIONS

The following table sets forth the percentage of revenue for certain items in our statements of operations for the periods indicated:

<TABLE>
<CAPTION>

	YEARS ENDED DECEMBER 31,		
	1997	1998	1999
<S>	<C>	<C>	<C>
Revenue	100.0%	100.0%	100.0%
Cost of revenue	59.2%	47.7%	43.0%
Gross profit	40.8%	52.3%	57.0%
Operating Expenses:			
Research and development	21.9%	21.0%	18.5%
Selling, general and administrative	38.6%	31.2%	31.7%
Contract termination and legal	99.5%	--	--
Net operating income (loss)	(119.2)%	0.1%	6.8%
Interest expense	(0.6)%	(0.5)%	(0.2)%
Interest income and other, net	1.6%	1.2%	1.4%
Net income (loss)	(118.2)%	0.8%	8.0%

</TABLE>

YEARS ENDED DECEMBER 31, 1997, 1998 AND 1999

REVENUE. Our revenue for 1997, 1998 and 1999 was $28.5 million, $30.0 million and $39.8 million, respectively, representing growth of 5.4% from 1997 to 1998 and 32.6% from 1998 to 1999. The 1998 revenue growth, as compared with 1997, reflected increasing sales of our pASIC 2 products as well as the initial shipments of our pASIC 3 products. The increase in 1998 was partially offset by declines in sales of our mature pASIC 1 products. In 1998, our pASIC 2 and pASIC 3 revenues together increased by approximately $3.8 million, while our pASIC 1 and other revenue declined by approximately $1.7 million and $0.6 million, respectively. The majority of the 1999 increase in revenue, as compared with 1998, was

due to growth in sales of our pASIC 3 products, the third generation of our FPGAs. Our pASIC 3 revenue increased in 1999 by approximately $4.6 million. In 1999, our pASIC 1 and pASIC 2 revenues together increased by approximately $3.0 million and revenue from our QuickRAM products, introduced in September 1998, increased by approximately $2.4 million. In aggregate, unit sales increased in both 1998 and 1999. The 1998 increase was partially offset by declining average selling prices of our pASIC 1 and pASIC 2 products. The 1999

increase was the result of higher unit sales and slightly higher average selling prices.

GROSS PROFIT. Gross profit was $11.6 million, $15.7 million and $22.7 million in 1997, 1998 and 1999, respectively, which was 40.8%, 52.3% and 57.0% of revenue for those periods. The increase in gross profit in 1998, as compared with 1997, was attributable to the growth in sales, the introduction of higher-margin pASIC 3 products, the absence of any inventory write-downs, and the maintenance of margin levels on our pASIC 1 and pASIC 2 products. The increase in 1999, as compared with 1998, was primarily due to the continued growth in sales and the introduction of higher-margin QuickRAM products. The 1999 increase was partially offset by a slight decrease in the average selling price of the older pASIC 1 and pASIC 2 product families.

RESEARCH AND DEVELOPMENT EXPENSE. Research and development expense was $6.2 million, $6.3 million, and $7.4 million in 1997, 1998 and 1999, respectively, which was 21.9%, 21.0% and 18.5% of revenue for those periods. The increase in research and development spending in 1999, as compared with 1998, was primarily due to an increase in the number of employees involved in research and development as we accelerated the introduction of new products, particularly our first ESPs.

SELLING, GENERAL AND ADMINISTRATIVE EXPENSE. Selling, general and administrative expense was $11.0 million, $9.4 million and $12.6 million in 1997, 1998 and 1999, respectively, which was 38.6%, 31.2% and 31.7% of revenue for those periods The decrease in selling, general and administrative expenses in 1998, as compared with 1997, was attributable to reduced personnel costs due to temporary vacancies in senior management positions. The increase in 1999, as compared with 1998, was primarily due to increased personnel costs.

CONTRACT TERMINATION AND LEGAL EXPENSE. We recorded an expense of $23.0 million in the first quarter of 1997 as a result of the termination of our 1992 agreement with Cypress. Legal and settlement costs associated with the Actel litigation were $5.3 million in 1997. No additional charges were recorded upon settlement of this litigation in 1998.

DEFERRED COMPENSATION. With respect to the grant of stock options to employees, we recorded aggregate deferred compensation of $1.9 million, $204,000 and $908,000 in 1997, 1998 and 1999, respectively. The amount of deferred compensation is presented as a reduction of stockholders' equity and amortized ratably over the vesting period of the applicable options, generally four years. We amortized $625,000, $426,000 and $512,000 in 1997, 1998 and 1999, respectively. The amortization of deferred compensation is recorded as research and development and selling, general and administrative expenses, depending on the related employees' activities.

INTEREST AND OTHER INCOME, NET. Interest and other income, net of expense, was $272,000, $203,000 and $452,000 in 1997, 1998 and 1999, respectively. Interest and other income decreased in 1998 as interest income on increased cash balances was offset by interest expense incurred as a result of new equipment financing arrangements. The increase in 1999 interest income was due mainly to our investment of proceeds from the October 1999 initial public offering.

PROVISION FOR INCOME TAXES

No provision for income taxes was recorded for the year ended December 31, 1997 as the Company incurred an operating loss. No provision for income taxes was recorded for the years ended December 31,

1998 and 1999, as we were able to utilize a portion of our state and federal net operating loss carryforwards and other tax attributes. At December 31, 1999, we had net operating loss carryforwards for federal and state tax purposes of approximately $42.0 million and $21.0 million, respectively. These carryforwards, if not utilized to offset future taxable income and income taxes payable, will begin to expire in 2000 and will continue to expire through 2017.

LIQUIDITY AND CAPITAL RESOURCES

We financed our operating loss in 1997 primarily through the issuance of common stock and the incurrence of debt to finance capital equipment purchases. We have been profitable since the third quarter of 1998. On October 15, 1999, we completed an initial public offering of our common stock in which we sold a total of 3,770,635 shares at $10.00 per share for total proceeds of $33.9 million, net of underwriting discounts, commissions and issuance costs. At December 31, 1999, we had $34.6 million in cash, an increase of $27.0 million

from cash held at December 31, 1998. This increase was due primarily to money received as part of our initial public offering. As of December 31, 1999, we had an accumulated deficit of $58.0 million.

We have an equipment financing line with a commercial bank. At December 31, 1999, we had obligations of $561,000 outstanding under this equipment line with no remaining available balance. The outstanding obligations under the equipment line are due over the next one to three years. The interest rate on these borrowings is at the bank's prime interest rate plus 0.25%.

Net cash provided by (used for) operating activities was $(1.4) million, $2.3 million and $(3.2) million in 1997, 1998 and 1999, respectively. The decrease in cash in 1997 was primarily attributable to increases in working capital, particularly accounts receivable and inventory. Inventory reductions were the primary source of cash in 1998. In 1999, we paid our remaining obligations to Actel per the August 1998 settlement agreement. Net income and an increase in accounts payable were the primary sources of cash in 1999. Our operating cash flow activities are affected by changes in our accounts receivable and related allowances. At December 31, 1997, 1998 and 1999 we had allowances for doubtful accounts totaling $245,000, $245,000 and $194,000, respectively. We have not had any material collection issues to date. At December 31, 1997, 1998 and 1999 we had sales returns and allowance reserves totaling $2.4 million, $3.0 million and $1.1 million, respectively, offsetting accounts receivable balances for contractual obligations for potential product returns and discounts. The change in the amount of sales returns and allowance reserves is due to the amount of credits earned but not yet taken by distributors.

Net cash used for investing activities was $2.6 million, $679,000 and $3.3 million in 1997, 1998 and 1999, respectively. All of this cash was used for the acquisition of property and equipment. The majority of the acquisitions in 1997 were financed under our equipment financing line. We intend to purchase approximately $5.0 million of additional capital assets during 2000.

Net cash provided by (used for) financing activities was $1.1 million, $(1.4) million, and $33.4 million in 1997, 1998 and 1999, respectively. The primary source of cash in 1997 was $1.5 million of borrowings from a bank which were used to acquire property and equipment. In 1999 the primary source of cash was the $33.9 million raised in the October 15, 1999 initial public offering. Cash was used to repay bank debt of $1.5 million, $1.5 million and $1.2 million in 1997, 1998 and 1999, respectively.

Our relationship with TSMC requires that we provide a forecast of the minimum level of our wafer requirements for the following year. This creates a minimum wafer purchase commitment to TSMC for such year. For 2000, our committed purchases from TSMC are $9.4 million. Our agreement with Cypress does not have similar minimum purchase commitments.

We require substantial working capital to fund our business, particularly to finance inventories and accounts receivable. Our future capital requirements will depend on many factors, including the rate of sales growth, market acceptance of our existing and new products, the amount and timing of research and

development expenditures, the timing of the introduction of new products and expansion of sales and marketing efforts. There can be no assurance that additional equity or debt financing, if required, will be available on satisfactory terms. We believe the net proceeds of this offering combined with existing capital resources and cash generated from operations will be sufficient to meet our needs for the next 12 months, although we could seek to raise additional capital during that period. After the next 12 months, our capital and operating requirements will depend on many factors, including the levels at which we maintain inventory and accounts receivable, costs of securing access to adequate manufacturing capacity and increases in our operating expenses.

On March 20, 2000, we filed a registration statement with the Securities and Exchange Commission for a proposed offering of 4,568,059 shares of our common stock. Of the shares included in the offering, it is expected that approximately 1,500,000 shares will be offered by us, and 3,068,059 shares will be offered for resale by selling stockholders.

INFLATION

The impact of inflation on our business has not been material for the fiscal years ended December 31, 1997, 1998 and 1999.

RECENTLY ISSUED ACCOUNTING PRONOUNCEMENTS

In December 1999, the Securities and Exchange Commission ("SEC") issued Staff Accounting Bulletin No. 101 ("SAB 101"), "Revenue Recognition in Financial Statements." SAB 101 summarizes certain of the SEC's views in applying generally accepted accounting principles to revenue recognition in financial statements. We are required to adopt SAB 101 in the first quarter of fiscal year 2000 and are currently studying the impact of SAB 101 on our financial statements. We do not believe that SAB 101 will have a material impact on our financial statements.

In June 1998, the Financial Accounting Standards Board issued Statement on Financial Accounting Standards No. 133, "Accounting for Derivative Instruments and Hedging Activities." SFAS No. 133 establishes a new model for accounting for derivatives and hedging activities and supersedes and amends a number of existing accounting standards. SFAS No. 133 requires that all derivatives be recognized in the balance sheet at their fair market value, and the corresponding derivative gains or losses be either reported in the statement of operations or as a deferred item depending on the type of hedge relationship that exists with respect to such derivative. SFAS No. 133, as amended by SFAS No. 137, "Accounting for Derivative Instruments and Hedging Activities--Deferral of Effective Date of FASB Statement No. 133," is effective for all fiscal quarters and years beginning after June 15, 2000. We do not currently have, or plan to enter into, forward exchange contracts to hedge exposures denominated in foreign currencies or any other derivative financial instruments for trading or speculative purposes.

YEAR 2000 COMPLIANCE

We are aware of the issues surrounding the year 2000 and problems relating to computers and computer software incorrectly distinguishing between 21st and 20th century dates. As a result, beginning on January 1, 2000, computer systems and software used by many companies and organizations in a wide variety of industries, including technology, transportation, utilities, finance and telecommunications, may have produced erroneous results or failed unless they had been modified or upgraded to process date information correctly. We have modified or replaced any software applications that had source code unable to process data information correctly. We addressed the Year 2000 preparedness of our critical suppliers and third party software providers. As of the date of this prospectus, we have not experienced any Year 2000 problems with our products, facilities, critical suppliers or vendors. We use software, computer technology and other services internally developed and provided by third-party vendors that may fail due to the Year 2000 phenomenon even after January 1, 2000. This failure may involve significant time and

expense, and uncorrected problems could seriously harm our business. In addition, the potential failure of our customers to ensure that their operations are Year 2000 compliant could have an adverse effect on them, which in turn could limit their ability to use our products and services or process our invoices in a timely manner.

Through December 31, 1999, we have incurred expenses of approximately $400,000 in addressing Year 2000 problems. We do not anticipate that we will incur any additional expenses relating to Year 2000 problems.

RISK FACTORS

OUR FUTURE OPERATING RESULTS ARE LIKELY TO FLUCTUATE AND THEREFORE MAY FAIL TO MEET EXPECTATIONS WHICH COULD CAUSE OUR STOCK PRICE TO DECLINE

Our operating results have varied widely in the past and are likely to do so in the future. In addition, our operating results may not follow any past trends. Our future operating results will depend on many factors and may fail to meet our expectations for a number of reasons, including those set forth in these risk factors. Any failure to meet expectations could cause our stock price to significantly fluctuate or decline.

Factors that could cause our operating results to fluctuate that relate to our internal operations include:

- the need for continual, rapid new product introductions;

- changes in our product mix; and

- our inability to adjust our fixed costs in the face of any declines in sales.

Factors that could cause our operating results to fluctuate that depend upon our suppliers and customers include:

- the timing of significant product orders, order cancellations and reschedulings;

- the availability of production capacity and fluctuations in the manufacturing yields at the facilities that manufacture our devices; and

- the cost of raw materials and manufacturing services from our suppliers.

Factors that could cause our operating results to fluctuate that are industry risks include:

- intense competitive pricing pressures;

- introductions of or enhancements to our competitors' products; and

- the cyclical nature of the semiconductor industry.

Our day-to-day business decisions are made with these factors in mind. Although certain of these factors are out of our immediate control, unless we can anticipate, and be prepared with contingency plans that respond to these factors, we will be unsuccessful in carrying out our business plan.

WE CANNOT ASSURE YOU THAT WE WILL REMAIN PROFITABLE BECAUSE WE HAVE A HISTORY OF LOSSES AND HAVE ONLY RECENTLY BECOME PROFITABLE

We incurred significant losses from our inception in 1988 through 1997. Our accumulated deficit as of December 31, 1999 was $58.0 million. We had net income of $3.2 million in 1999. We cannot assure you that we will be profitable in any future periods and you should not rely on the historical growth of our revenue and our recent profitability as any indication of our future operating results or prospects.

IF WE FAIL TO SUCCESSFULLY DEVELOP, INTRODUCE AND SELL NEW PRODUCTS, WE MAY BE UNABLE TO COMPETE EFFECTIVELY IN THE FUTURE

We operate in a highly competitive, quickly changing environment marked by rapid obsolescence of existing products. Our future success depends on our ability to develop, introduce and successfully market new products, including embedded standard products, or ESPs. We introduced our ESPs in September 1998. To date, we have been selling our ESPs in limited quantities, and revenue from our ESPs has been very small. If any of the following occur, our business will be materially harmed:

- we fail to complete and introduce new product designs in a timely manner;

- we are unable to have these new products manufactured according to design specifications;

- our customers do not successfully introduce new systems or products incorporating our products;

- our sales force and independent distributors do not create adequate demand for our products; or

- market demand for our new products, such as ESPs, does not develop as anticipated.

WE HAVE ONLY RECENTLY INTRODUCED OUR EMBEDDED STANDARD PRODUCTS; THEREFORE, WE CANNOT ACCURATELY PREDICT THEIR FUTURE LEVEL OF ACCEPTANCE BY OUR CUSTOMERS, AND WE MAY NOT BE ABLE TO GENERATE ANTICIPATED REVENUE FROM THESE PRODUCTS

We have only recently started selling embedded standard products. In 1999, ESPs accounted for approximately 6.3% of our revenue. We do not know the extent to which systems manufacturers will purchase or utilize our ESPs. Since we anticipate that ESPs will become an increasingly larger component of our business, their failure to gain acceptance with our customers would materially harm our business. We cannot assure you that our ESPs will be commercially successful or that these products will result in significant additional revenues

or improved operating margins in future periods.

IF THE MARKET IN WHICH WE SELL OUR EMBEDDED STANDARD PRODUCTS DOES NOT GROW AS WE ANTICIPATE, IT WILL MATERIALLY AND ADVERSELY AFFECT OUR ANTICIPATED REVENUE

The market for embedded standard products is relatively new and still emerging. If this market does not grow at the rate we anticipate, our business will be materially harmed. One of the reasons that this market might not grow as we anticipate is that many systems manufacturers are not yet fully aware of the benefits provided by embedded standard products, in general, or the benefits of our ESPs, specifically. Additionally, systems manufacturers may use existing technologies other than embedded standard products or yet to be introduced technologies to satisfy their needs. Although we have devoted and intend to continue to devote significant resources promoting market awareness of the benefits of embedded standard products, our efforts may be unsuccessful or insufficient.

WE EXPEND SUBSTANTIAL RESOURCES IN DEVELOPING AND SELLING OUR PRODUCTS, AND WE MAY BE UNABLE TO GENERATE SIGNIFICANT REVENUE AS A RESULT OF THESE EFFORTS

To establish market acceptance of our products, we must dedicate significant resources to research and development, production and sales and marketing. We experience a long delay between the time when we expend these resources and the time when we begin to generate revenue, if any, from these expenditures. Typically, this delay is one year or more. We record as expenses the costs related to the development of new semiconductor products and software as these expenses are incurred. As a result, our profitability from quarter to quarter and from year to year may be materially and adversely affected by the number and timing of our new product introductions in any period and the level of acceptance gained by these products.

OUR CUSTOMERS MAY CANCEL OR CHANGE THEIR PRODUCT PLANS AFTER WE HAVE EXPENDED SUBSTANTIAL TIME AND RESOURCES IN THE DESIGN OF THEIR PRODUCTS

If one of our potential customers cancels, reduces or delays product orders from us or chooses not to release equipment that incorporates our products after we have spent substantial time and resources in designing a product, our business could be materially harmed. Our customers often evaluate our products for six to twelve months or more before designing them into their systems, and they may not commence volume shipments for up to an additional six to twelve months, if at all. During this lengthy sales cycle, our potential customers may also cancel or change their product plans. Even when customers incorporate one or more of our products into their systems, they may ultimately discontinue the shipment of their systems that incorporate our products. Customers whose products achieve high volume production may choose to replace our products with lower cost customized semiconductors.

WE WILL BE UNABLE TO COMPETE EFFECTIVELY IF WE FAIL TO ANTICIPATE PRODUCT OPPORTUNITIES BASED UPON EMERGING TECHNOLOGIES AND STANDARDS AND FAIL TO DEVELOP PRODUCTS THAT INCORPORATE THESE TECHNOLOGIES AND STANDARDS

We may spend significant time and money on research and development to design and develop products around an emerging technology or industry standard. To date, we have introduced only one product family, QuickPCI, that is designed to support a specific industry standard. If an emerging technology or industry standard that we have identified fails to achieve broad market acceptance in our target markets, we may be unable to generate significant revenue from our research and development efforts. Moreover, even if we are able to develop products using adopted standards, our products may not be accepted in our target markets. As a result, our business would be materially harmed.

We have limited experience in designing and developing products that support industry standards. If systems manufacturers move away from the use of industry standards that we support with our products and adopt alternative standards, we may be unable to design and develop new products that conform to these new standards. The expertise required is unique to each industry standard, and we would have to either hire individuals with the required expertise or acquire such expertise through a licensing arrangement or by other means. The demand for individuals with the necessary expertise to develop a product relating to a particular industry standard is generally high, and we may not be able to hire such individuals. The cost to acquire such expertise through licensing or other means may be high and such arrangements may not be possible in a timely manner, if at all.

WE MAY ENCOUNTER PERIODS OF INDUSTRY-WIDE SEMICONDUCTOR OVERSUPPLY, RESULTING IN PRICING PRESSURE AND UNDERUTILIZATION OF MANUFACTURING CAPACITY, AS WELL AS UNDERSUPPLY, RESULTING IN A RISK THAT WE COULD BE UNABLE TO FULFILL OUR CUSTOMERS' REQUIREMENTS

The semiconductor industry has historically been characterized by wide fluctuations in the demand for, and supply of, its products. These fluctuations have resulted in circumstances when supply and demand for the industry's products have been widely out of balance. Our operating results may be materially harmed by industry-wide semiconductor oversupply, which could result in severe pricing pressure and underutilization of our manufacturing capacity. In a market with undersupply, we would have to compete with larger foundry customers for limited manufacturing capacity. In such an environment, we may be unable to have our products manufactured in a timely manner or in quantities necessary to meet our requirements. Since we outsource all of our manufacturing, we are particularly vulnerable to such supply shortages. As a result, we may be unable to fulfill orders and may lose customers. Any future industry-wide oversupply or undersupply of semiconductors would materially harm our business.

NONE OF OUR PRODUCTS IS CURRENTLY MANUFACTURED BY MORE THAN ONE MANUFACTURER, WHICH EXPOSES US TO THE RISK OF HAVING TO IDENTIFY AND QUALIFY ONE OR MORE SUBSTITUTE SUPPLIERS

We depend upon independent third parties to manufacture, assemble and test our semiconductor products. None of our products is currently manufactured by more than one manufacturer. We have contractual arrangements with our two foundry manufacturers of semiconductors, Taiwan Semiconductor Manufacturing Company and Cypress Semiconductor Corporation, to provide us with specified manufacturing capacity. Our assembly and test work is done on a purchase order basis. If we are unable to secure adequate manufacturing capacity from TSMC, Cypress or other suppliers to meet our supply requirements, our business will be materially harmed. Processes used to manufacture our products are complex, customized to our specifications and can only be performed by a limited number of manufacturing facilities. If our current manufacturing suppliers are unable to provide us with adequate manufacturing capacity, we would have to identify and qualify one or more substitute suppliers for a substantial majority of our products. Our manufacturers may experience unanticipated events, like the September 1999 Taiwan earthquake, that could inhibit their abilities to provide us with adequate manufacturing capacity on a timely basis, or at all. Introducing new products or transferring existing products to a new third party manufacturer would require significant development time to adapt our designs to their manufacturing processes and could cause product shipment delays. In addition, the costs associated with manufacturing our products may increase if we are required to use a new third party manufacturer. If we fail to satisfy our manufacturing requirements, our business would be materially harmed.

IF WE FAIL TO ADEQUATELY FORECAST DEMAND FOR OUR PRODUCTS, WE MAY INCUR PRODUCT SHORTAGES OR EXCESS PRODUCT INVENTORY.

Our agreements with third-party manufacturers require us to provide forecasts of our anticipated manufacturing orders, and place binding manufacturing orders in advance of receiving purchase orders from our customers. This may result in product shortages or excess product inventory because we are not permitted to increase or decrease our rolling forecasts under such agreements. Obtaining additional supply in the face of product shortages may be costly or not possible, especially in the short term. Our failure to adequately forecast demand for our products would materially harm our business.

FLUCTUATIONS IN OUR PRODUCT YIELDS, ESPECIALLY OUR NEW PRODUCTS, MAY INCREASE THE COSTS OF OUR MANUFACTURING PROCESS.

Difficulties in the complex semiconductor manufacturing process can render a substantial percentage of semiconductor wafers nonfunctional. We have, in the past, experienced manufacturing runs that have contained substantially reduced or no functioning devices. Varying degrees of these yield reductions occur frequently in our manufacturing process. These yield reductions, which can occur without warning, may result in substantially higher manufacturing costs and inventory shortages to us. We may experience yield problems in the future which may materially harm our business. In addition, yield problems may take a significant period of time to analyze and correct. Our reliance on third party suppliers may extend the period of time required to analyze and correct these problems. As a result, if we are unable to respond rapidly to market demand, our business would suffer.

Yield reductions frequently occur in connection with the manufacture of newly introduced products. Newly introduced products, such as our QuickPCI family of ESPs, are often more complex and more difficult to produce, increasing the risk of manufacturing-related defects. While we test our products, these products may still contain errors or defects that we find only after we have commenced commercial production. Our customers may not place new orders for our products if the products have reliability problems, which would materially harm our business.

WE MAY BE UNABLE TO GROW OUR BUSINESS IF THE MARKETS IN WHICH OUR CUSTOMERS SELL THEIR PRODUCTS DO NOT GROW

Our success depends in large part on the continued growth of various markets that use our products. Any decline in the demand for our products in the following markets could materially harm our business:

- telecommunications and data communications;

- video/audio, graphics and imaging;

- instrumentation and test;

- high-performance computing; or

- military systems.

Slower growth in any of the other markets in which our products are sold may also materially harm our business. Many of these markets are characterized by rapid technological change and intense competition. As a result, systems sold by our customers that use our products may face severe price competition, become obsolete over a short time period, or fail to gain market acceptance. Any of these occurrences would materially harm our business.

IN ORDER TO REMAIN PROFITABLE, WE WILL NEED TO OFFSET THE GENERAL PATTERN OF DECLINES AND FLUCTUATIONS IN THE PRICES OF OUR PRODUCTS

The average selling prices of our products historically have declined during the products' lives by, on average, approximately 7% per year, and we expect this trend to continue. If we are unable to achieve cost reductions, increase unit demand or introduce new higher-margin products in a timely manner to offset these price declines, our business would be materially harmed.

In addition, the selling prices for our products fluctuate significantly with real and perceived changes in the balance of supply and demand for our products and comparable products. The growth in the worldwide supply of field programmable gate arrays in recent periods has added to the decrease in the average selling prices for our products. In addition, we expect our competitors to invest in new manufacturing process technologies and achieve significant manufacturing yield improvements in the future. These developments could increase the worldwide supply of field programmable gate arrays and alternate products and create additional downward pressure on pricing. If the worldwide supply of field programmable gate arrays grows faster than the demand for such products in the future, the price for which we can sell such products may decline, which would materially harm our business.

WE DEPEND UPON THIRD PARTY DISTRIBUTORS TO MARKET AND SELL OUR PRODUCTS, AND THEY MAY DISCONTINUE SALE OF OUR PRODUCTS, FAIL TO GIVE OUR PRODUCTS PRIORITY OR BE UNABLE TO SUCCESSFULLY MARKET, SELL AND SUPPORT OUR PRODUCTS

We employ independent, third-party distributors to market and sell a significant portion of our products. During 1999, approximately 80% of our sales were made through our distributors. We rely on four principal distributors to market and sell a majority of our products, particularly in North America. Although we have contracts with our distributors, any of them may terminate their relationship with us on short notice. The loss of one or more of our principal distributors, or our inability to attract new distributors, would materially harm our business. We may lose distributors in the future and we may be unable to recruit additional or replacement distributors. As a result, our future performance will depend in part on our ability to retain our existing distributors and attract new distributors that will be able to market, sell and support our products effectively.

Many of our distributors, including our principal distributors, market and sell products for other companies, and many of these products may compete directly or indirectly with our products. We generally

are not one of the principal suppliers of products to our distributors. If our distributors give higher priority or greater attention to the products of other companies, including products that compete with our products, our business would be materially harmed.

WE MAY BE UNABLE TO ACCURATELY PREDICT QUARTERLY RESULTS IF DISTRIBUTORS ARE INACCURATE OR UNTIMELY IN PROVIDING US WITH THEIR RESALE REPORTS, WHICH COULD ADVERSELY AFFECT THE TRADING PRICE OF OUR STOCK

Since we generally recognize revenue from sales to our distributors only when these distributors make sales to customers, we are highly dependent on the accuracy and timeliness of their resale reports. Inaccurate resale reports contribute to our difficulty in predicting and reporting our quarterly revenue and results of operations, particularly in the last month of the quarter. If we fail to accurately predict our revenue and results of operations on a quarterly basis, our stock price could materially fluctuate. Distributors occasionally increase their inventories of our products in anticipation of growth in the demand for our products. If this growth does not occur, distributors will decrease their orders for our products in subsequent periods, and our business would be materially harmed.

CUSTOMERS MAY CANCEL OR DEFER SIGNIFICANT PURCHASE ORDERS OR OUR DISTRIBUTORS MAY RETURN OUR PRODUCTS, WHICH WOULD CAUSE OUR INVENTORY LEVELS TO INCREASE AND OUR REVENUES TO DECLINE

We sell our products on a purchase order basis through our distributors and direct sales channels, and our distributors or customers may cancel purchase orders at any time with little or no penalty. In addition, our distributor agreements generally permit our distributors to return unprogrammed products to us. Contractually, our distributors are permitted to return up to 10%, by value, of the products they purchase from us every six months. In early 1998, for example, a distributor cancelled a significant purchase order as a result of a customer switching from a product we supply to a competitor's product. The distributor also returned a significant amount of inventory of the product to us, which took approximately 18 months for us to resell. If our customers cancel or defer significant purchase orders or our distributors return our products, our inventories would increase, which would materially harm our business.

MANY SYSTEMS MANUFACTURERS MAY BE UNWILLING TO SWITCH TO OUR PRODUCTS BECAUSE OF THEIR FAMILIARITY WITH THE PRODUCTS OFFERED BY OUR DIRECT COMPETITORS SUCH AS XILINX AND ALTERA, WHICH DOMINATE THE PROGRAMMABLE LOGIC MARKET

The semiconductor industry is intensely competitive and characterized by:

- erosion of selling prices over product lives;

- rapid technological change;

- short product life cycles; and

- strong domestic and foreign competition.

If we are not able to compete successfully in this, environment, our business will be materially harmed. A primary cause of this highly competitive environment is the strengths of our competitors. Our industry consists of major domestic and international semiconductor companies, many of which have substantially greater financial, technical, marketing, distribution and other resources than we do. Our current direct competitors include suppliers of complex programmable logic devices and field programmable gate arrays, such as Xilinx, Altera, Actel, Lattice Semiconductor and Lucent. Xilinx and Altera together have a majority share of the programmable logic market. Many systems manufacturers may be unwilling or unable to switch to our products due to their familiarity with competitors' products or other inhibiting factors.

We also face competition from companies that offer application specific integrated circuits, which may be obtained at lower costs for higher volumes and typically have greater logic capacity, additional features and higher performance than those of our products. We may also face competition from suppliers of

products based on new or emerging technologies, including ESPs. Our inability to successfully compete in any of the following areas could materially harm our

business:

- the development of new products and manufacturing technologies;

- the quality and price of products and devices;

- the diversity of product lines; or

- the cost effectiveness of design, development, manufacturing and marketing efforts.

WE MAY BE UNABLE TO SUCCESSFULLY MANAGE OUR GROWTH IF WE FAIL TO COMPETE EFFECTIVELY WITH OTHERS TO ATTRACT AND RETAIN KEY PERSONNEL

We believe our future success will depend upon our ability to successfully manage our growth, including attracting and retaining engineers and other highly skilled personnel. Our employees are at-will and not subject to employment contracts. Hiring qualified sales and technical personnel will be difficult due to the limited number of qualified professionals. Competition for these types of employees is intense. We have in the past experienced difficulty in recruiting and retaining qualified sales and technical personnel. For example, in the past 18 months, two of our executive officers resigned to pursue other opportunities. Failure to attract and retain personnel, particularly sales and technical personnel, would materially harm our business.

As we seek to expand our operations, we may also significantly strain our management and financial systems and other resources. We cannot be certain that our systems, procedures, controls and existing space will be adequate to support our operations.

WE MAY BE UNABLE TO ADEQUATELY PROTECT OUR INTELLECTUAL PROPERTY RIGHTS, AND MAY FACE SIGNIFICANT EXPENSES AS A RESULT OF FUTURE LITIGATION

Protection of intellectual property rights is crucial to our business, since that is how we keep others from copying the innovations which are central to our existing and future products. From time to time, we receive letters alleging patent infringement or inviting us to take a license to other parties' patents. We evaluate these letters on a case-by-case basis. In September 1999, we received an offer to license a patent related to field programmable gate array architecture. We have not yet determined whether this license would be necessary or useful, or whether a license would be obtainable at a reasonable price. Offers such as these may lead to litigation if we reject the opportunity to obtain the license. We have in the past and may again become involved in litigation relating to alleged infringement by us of others' patents or other intellectual property rights. This kind of litigation is expensive to all parties and consumes large amounts of management's time and attention. For example, we incurred substantial costs associated with the litigation and settlement of our dispute with Actel Corporation, which materially harmed our business. In addition, if the September 1999 letter or other similar matters result in litigation that we lose, a court could order us to pay substantial damages and/or royalties, and prohibit us from making, using, selling or importing essential technologies. For these and other reasons, this kind of litigation would materially harm our business. Also, although we may seek to obtain a license under a third party's intellectual property rights in order to bring an end to certain claims or actions asserted against us, we may not be able to obtain such a license on reasonable terms or at all.

We have entered into technology license agreements with third parties which give those parties the right to use patents and other technology developed by us, and which give us the right to use patents and other technology developed by them. We anticipate that we will continue to enter into these kinds of licensing arrangements in the future; however, it is possible that desirable licenses will not be available to us on commercially reasonable terms. If we lose existing licenses to key technology, or are unable to enter into new licenses which we deem important, it could materially harm our business, and materially and adversely affect our business.

Because it is critical to our success that we are able to prevent competitors from copying our innovations, we intend to continue to seek patent and trade secret protection for our products. The process of seeking patent protection can be long and expensive, and we cannot be certain that any currently pending or future applications will actually result in issued patents, or that, even if patents are issued, they will be of sufficient scope or strength to provide meaningful protection or any commercial advantage to us. Furthermore, others may develop technologies that are similar or superior to our

technology or design around the patents we own. We also rely on trade secret protection for our technology, in part through confidentiality agreements with our employees, consultants and third parties. However, employees may breach these agreements, and we may not have adequate remedies for any breach. In any case, others may come to know about or determine our trade secrets through a variety of methods. In addition, the laws of certain territories in which we develop, manufacture or sell our products may not protect our intellectual property rights to the same extent as do the laws of the United States.

PROBLEMS ASSOCIATED WITH INTERNATIONAL BUSINESS OPERATIONS COULD AFFECT OUR ABILITY TO MANUFACTURE AND SELL OUR PRODUCTS

Most of our products are manufactured outside of the United States at manufacturing facilities operated by our suppliers in Taiwan, South Korea and the Philippines. As a result, our manufacturing operations are subject to risks of political instability, including the risk of conflict between Taiwan and the People's Republic of China and conflict between North Korea and South Korea. Moreover, the majority of available manufacturing capacity for our products is located in Taiwan and South Korea.

Sales to customers located outside the United States accounted for 43%, 47% and 48% of our total sales in 1997, 1998 and 1999, respectively. We anticipate that sales to customers located outside the United States will continue to represent a significant portion of our total sales in future periods and the trend of foreign customers accounting for an increasing portion of our total sales may continue. In addition, most of our domestic customers sell their products outside of North America, thereby indirectly exposing us to risks associated with foreign commerce. Asian economic instability could also materially and adversely affect our business, particularly to the extent that this instability impacts the sales of products manufactured by our customers. Accordingly, our operations and revenues are subject to a number of risks associated with foreign commerce, including the following:

- managing foreign distributors;

- staffing and managing foreign branch offices;

- political and economic instability;

- foreign currency exchange fluctuations;

- changes in tax laws, tariffs and freight rates;

- timing and availability of export licenses;

- inadequate protection of intellectual property rights in some countries; and

- obtaining governmental approvals for certain products.

In the past we have denominated sales of our products in foreign countries exclusively in U.S. dollars. As a result, any increase in the value of the U.S. dollar relative to the local currency of a foreign country will increase the price of our products in that country so that our products become relatively more expensive to customers in the local currency of that foreign country. As a result, sales of our products in that foreign country may decline. To the extent any such risks materialize, our business would be materially harmed.

OUR PRINCIPAL STOCKHOLDERS HAVE SIGNIFICANT VOTING POWER AND MAY VOTE FOR ACTIONS THAT MAY NOT BE IN THE BEST INTERESTS OF OUR STOCKHOLDERS

Our officers, directors and principal stockholders together control approximately 51.23% of our outstanding common stock. As a result, these stockholders, if they act together, will be able to significantly influence the management and affairs of QuickLogic and all matters requiring stockholder approval, including the election of directors and approval of significant corporate transactions. This concentration of ownership may have the effect of delaying or preventing a change in control and might affect the market price of our common stock. This concentration of ownership may not be in the best interest of our other stockholders.

OUR CERTIFICATE OF INCORPORATION AND BYLAWS AND DELAWARE LAW CONTAIN PROVISIONS THAT COULD DISCOURAGE A TAKEOVER

Our basic corporate documents and Delaware law contain provisions that might

enable our management to resist a takeover. These provisions might discourage, delay or prevent a change in the control of QuickLogic or a change in our management. Our certificate of incorporation provides that we will have a classified board of directors, with each class of directors subject to re-election every three years. This classified board when implemented will have the effect of making it more difficult for third parties to insert their representatives on our board of directors and gain control of QuickLogic. These provisions could also discourage proxy contests and make it more difficult for you and other stockholders to elect directors and take other corporate actions. The existence of these provisions could limit the price that investors might be willing to pay in the future for shares of the common stock.

Our certificate of incorporation also provides that our board of directors may, without further action by the stockholders, issue shares of preferred stock in one or more series and fix the rights, preferences, privileges and restrictions thereof. The issuance of preferred stock could adversely affect the voting power of holders of common stock and the likelihood that such holders will receive dividend payments and payments upon liquidation. In addition, the issuance of preferred stock could have the effect of delaying, deferring or preventing a change in control of QuickLogic. We have no present plan to issue any shares of preferred stock.

ITEM 7A. QUANTITATIVE AND QUALITATIVE DISCLOSURES ABOUT MARKET RISK

INTEREST RATE RISK

We do not use derivative financial instruments in our investment portfolio. Our investment portfolio is generally comprised of commercial paper. We place investments in instruments that meet high credit quality standards. These securities are subject to interest rate risk, and could decline in value if interest rates fluctuate. Due to the short duration and conservative nature of our investment portfolio, we do not expect any material loss with respect to our investment portfolio. A 10% move in interest rates as of December 31, 1999 would have an immaterial effect on our pretax earnings and the carrying value of its investments over the next fiscal year.

FOREIGN CURRENCY EXCHANGE RATE RISK

All of the Company's sales, cost of manufacturing and marketing are transacted in U.S. dollars. Accordingly, our results of operations are not subject to foreign exchange rate fluctuations.

ITEM 8. FINANCIAL STATEMENTS AND SUPPLEMENTARY DATA

INDEX TO CONSOLIDATED FINANCIAL STATEMENTS

<TABLE>
<CAPTION>

</TABLE>

REPORT OF INDEPENDENT ACCOUNTANTS

To the Board of Directors and Stockholders of
QuickLogic Corporation

In our opinion, the accompanying consolidated balance sheets and the related

consolidated statements of operations, of stockholders' equity (deficit) and of cash flows present fairly, in all material respects, the financial position of QuickLogic Corporation and its subsidiary at December 31, 1999 and 1998, and the results of their operations and their cash flows for each of the three years in the period ended December 31, 1999, in conformity with accounting principles generally accepted in the United States. In addition, in our opinion, the consolidated financial statement schedules listed in the index appearing under item 14(a)2 present fairly, in all material respects, the information set forth therein when read in conjunction with the related financial statements. These financial statements and financial statement schedules are the responsibility of the Company's management; our responsibility is to express an opinion on these financial statements and financial statement schedules based on our audits. We conducted our audits of these statements in accordance with auditing standards generally accepted in the United States, which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for the opinion expressed above.

PricewaterhouseCoopers LLP
San Jose, California
January 25, 2000

QUICKLOGIC CORPORATION

CONSOLIDATED BALANCE SHEET

(IN THOUSANDS, EXCEPT PER SHARE AMOUNTS)

<TABLE>
<CAPTION>

	YEARS ENDED DECEMBER 31,	
	1998	1999
<S>	<C>	<C>
ASSETS		
Current assets:		
Cash and cash equivalents	$ 7,595	$ 34,558
Accounts receivable, net of allowances for doubtful accounts and sales returns and allowances of $3,272 and $1,305	2,031	5,543
Inventory	2,877	4,349
Other current assets	730	1,467
Total current assets	13,233	45,917
Property and equipment, net	2,892	4,510
Other assets	43	55
	$ 16,168	$ 50,482
LIABILITIES AND STOCKHOLDERS' EQUITY (DEFICIT)		
Trade payables	$ 2,204	$ 5,202
Accrued liabilities	2,425	2,405
Deferred income on shipments to distributors	4,737	5,026
Current portion of long-term obligations	7,186	716
Total current liabilities	16,552	13,349
Long-term obligations	591	128
	17,143	13,477
Commitments and contingencies (Notes 11 and 12)		
Stockholders' equity (deficit)		
Preferred stock, $0.001 par value; 61,568 and 10,000 shares authorized; 9,912 and no shares issued and outstanding	10	--
Common stock, $0.001 par value; 105,000 and 100,000 shares		

authorized, 4,279 and 18,102 shares outstanding.....	4	18
Additional paid-in capital.....	61,388	96,599
Stockholder note receivable.....	(121)	(121)
Deferred compensation.....	(1,084)	(1,480)
Accumulated deficit.....	(61,172)	(58,011)
Total stockholders' equity (deficit).....	(975)	37,005
	$ 16,168	$ 50,482

</TABLE>

The accompanying notes form an integral part of these Consolidated Financial Statements

QUICKLOGIC CORPORATION

CONSOLIDATED STATEMENT OF OPERATIONS

(IN THOUSANDS, EXCEPT PER SHARE AMOUNTS)

<TABLE>
<CAPTION>

	YEARS ENDED DECEMBER 31,		
	1997	1998	1999
<S>	<C>	<C>	<C>
Revenue.....	$ 28,460	$30,007	$39,785
Cost of revenue.....	16,855	14,303	17,103
Gross profit.....	11,605	15,704	22,682
Operating expenses:			
Research and development.....	6,235	6,294	7,355
Selling, general and administrative.....	10,981	9,368	12,618
Contract termination and legal.....	28,309	--	--
Net operating income (loss).....	(33,920)	42	2,709
Interest expense.....	(162)	(161)	(97)
Interest income and other, net.....	434	364	549
Net income (loss).....	$(33,648)	$ 245	$ 3,161
Net income (loss) per share:			
Basic.....	$ (10.41)	$ 0.06	$ 0.42
Diluted.....	$ (10.41)	$ 0.02	$ 0.19
Weighted average shares:			
Basic.....	3,232	4,231	7,615
Diluted.....	3,232	14,645	16,400

</TABLE>

The accompanying notes form an integral part of these Consolidated Financial Statements

QUICKLOGIC CORPORATION
CONSOLIDATED STATEMENT OF STOCKHOLDERS' EQUITY (DEFICIT)
(IN THOUSANDS)

<TABLE>
<CAPTION>

	CONVERTIBLE PREFERRED STOCK		COMMON STOCK		COMMON STOCK TO BE ISSUED		ADDITIONAL PAID-IN	STOCKHOLDER NOTE
	SHARES	AMOUNT	SHARES	AMOUNT	SHARES	AMOUNT	CAPITAL	RECEIVABLE
<S>	<C>	<C>	<C>	<C>	<C>	<C>	<C>	<C>
Balance at December 31, 1996.....	9,793	$ 10	828	$ 1	--	$ --	$40,484	$(119)
Common stock issued under stock option plan, net of repurchases.....	--	--	331	--	--	--	280	--
Issuance of Series F preferred stock for cash, net of issuance cost.....	119	--	--	--	--	--	781	--
Common stock to be issued in								

exchange for contract termination.....	--	--	--	--	3,038	18,409	--	--
Deferred compensation, net of terminations.....	--	--	--	--	--	--	1,890	--
Amortization of deferred compensation.....	--	--	--	--	--	--	--	--
Note receivable from stockholder.....	--	--	--	--	--	--	--	(2)
Net loss.....	--	--	--	--	--	--	--	--
Balance at December 1997.....	9,912	10	1,159	1	3,038	18,409	43,435	(121)
Common stock issued under stock option plan, net of repurchases.....	--	--	82	--	--	--	110	--
Common stock issued in exchange for contract termination.....	--	--	3,038	3	(3,038)	(18,409)	18,406	--
Deferred compensation, net of terminations.....	--	--	--	--	--	--	(563)	--
Amortization of deferred compensation.....	--	--	--	--	--	--	--	--
Net income.....	--	--	--	--	--	--	--	--
Balance at December 31, 1998.....	9,912	10	4,279	4	--	--	61,388	(121)
Common stock issued under stock option plan, net of repurchases.....	--	--	140	--	--	--	431	--
Deferred compensation, net of terminations.....	--	--	--	--	--	--	908	--
Amortization of deferred compensation.....	--	--	--	--	--	--	--	--
Conversion from preferred stock to common stock.....	(9,912)	(10)	9,912	10	--	--	--	--
Issuance of shares in connection with initial public offering, net of expenses $1,190.....	--	--	3,771	4	--	--	33,872	--
Net income.....	--	--	--	--	--	--	--	--
Balance at December 31, 1999.....	--	$ --	18,102	$18	--	$ --	$96,599	$(121)

<CAPTION>

	DEFERRED COMPENSATION	ACCUMULATED DEFICIT	TOTAL STOCKHOLDERS' EQUITY (DEFICIT)
<S>	<C>	<C>	<C>
Balance at December 31, 1996.....	$ (808)	$(27,769)	$ 11,799
Common stock issued under stock option plan, net of repurchases.....	--	--	280
Issuance of Series F preferred stock for cash, net of issuance cost.....	--	--	781
Common stock to be issued in exchange for contract termination.....	--	--	18,409
Deferred compensation, net of terminations.....	(1,890)	--	--
Amortization of deferred compensation.....	625	--	625
Note receivable from stockholder.....	--	--	(2)
Net loss.....	--	(33,648)	(33,648)
Balance at December 1997.....	(2,073)	(61,417)	(1,756)
Common stock issued under stock option plan, net of repurchases.....	--	--	110
Common stock issued in exchange for contract termination.....	--	--	--
Deferred compensation, net of terminations.....	563	--	--
Amortization of deferred compensation.....	426	--	426

Net income.....	--	245	245
Balance at December 31, 1998.....	(1,084)	(61,172)	(975)
Common stock issued under stock option plan, net of repurchases.....	--	--	431
Deferred compensation, net of terminations.....	(908)	--	--
Amortization of deferred compensation.....	512	--	512
Conversion from preferred stock to common stock.....	--	--	--
Issuance of shares in connection with initial public offering, net of expenses $1,190.....	--	--	33,876
Net income.....	--	3,161	3,161
Balance at December 31, 1999.....	$(1,480)	$(58,011)	$ 37,005

</TABLE>

QUICKLOGIC CORPORATION

CONSOLIDATED STATEMENT OF CASH FLOWS

(IN THOUSANDS)

<TABLE>
<CAPTION>

	YEAR ENDED DECEMBER 31,		
	1997	1998	1999
<S>	<C>	<C>	<C>
Cash flows from operating activities:			
Net income (loss).....	$(33,648)	$ 245	$ 3,161
Adjustments to reconcile net income (loss) to net cash provided by (used for) operating activities:			
Depreciation and other non-cash charges.....	817	1,322	1,636
Provision for doubtful accounts and sales returns.....	6,001	5,031	7,099
Amortization of deferred compensation.....	625	426	512
Gain on disposal of assets.....	--	(5)	--
Contract termination and other.....	28,309	--	--
Changes in assets and liabilities:			
Accounts receivable.....	(6,284)	(4,170)	(10,611)
Inventory.....	(1,225)	2,992	(1,472)
Other assets.....	(253)	(444)	(749)
Accounts payable.....	(243)	(597)	2,998
Accrued liabilities and other obligations.....	4,453	(2,477)	(5,731)
Net cash provided by (used for) operating activities.....	(1,448)	2,323	(3,157)
Cash flows from investing activities:			
Capital expenditures for property and equipment, net of dispositions.....	(2,639)	(679)	(3,254)
Cash flows from financing activities:			
Payment of long-term obligations.....	(1,473)	(1,490)	(1,183)
Proceeds from issuance of common stock, net.....	280	110	34,307
Proceeds from issuance of preferred stock, net.....	781	--	--
Note receivable from stockholder.....	(2)	--	--
Proceeds from bank borrowings.....	1,496	--	250
Net cash provided by (used for) financing activities.....	1,082	(1,380)	33,374
Net increase (decrease) in cash.....	(3,005)	264	26,963
Cash at beginning of period.....	10,336	7,331	7,595
Cash at end of period.....	$ 7,331	$ 7,595	$ 34,558

Non-cash transactions:

Inventory acquired in exchange for note payable.....	$ 1,396	$ --	$ --

</TABLE>

The accompanying notes form an integral part of these Consolidated Financial Statements

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

NOTE 1--THE COMPANY AND BASIS OF PRESENTATION

QuickLogic Corporation ("QuickLogic" or "the Company"), founded in 1988, operates in a single industry segment where it designs, develops, markets and supports advanced field programmable gate array semiconductors ("FPGAs"), embedded standard products ("ESPs") and associated software tools.

Our fiscal year ends on the Sunday closest to December 31. For presentation purposes, the financial statements and notes have been presented as ending on the last day of the nearest calendar month.

PRINCIPLES OF CONSOLIDATION

The consolidated financial statements include the accounts of QuickLogic Corporation and its wholly-owned subsidiary, QuickLogic International, Inc. All significant intercompany accounts and transactions are eliminated in consolidation.

USES OF ESTIMATES

The preparation of these financial statements in conformity with generally accepted accounting principles requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities as of the date of the financial statements and the reported amounts of revenues and expenses during the reporting period. Actual results could vary from those estimates, particularly in relation to sales returns and allowances, and product obsolescence.

NOTE 2--SIGNIFICANT ACCOUNTING POLICIES

CASH EQUIVALENTS AND SHORT-TERM INVESTMENTS

All highly-liquid investments purchased with a remaining maturity of three months or less are considered cash equivalents.

FAIR VALUE OF FINANCIAL INSTRUMENTS

The estimated fair value of financial instruments are determined by using available market information and appropriate valuation methodologies. However, considerable judgment is required to interpret and analyze the available data and to develop estimates. Accordingly, estimates could differ significantly from the amounts we would realize in a current market exchange. The estimated fair value of all financial instruments at December 31, 1997, 1998 and 1999, approximate the amounts presented in the balance sheets, due primarily to the short-term nature of these instruments.

FOREIGN CURRENCY TRANSACTIONS

We exclusively use the U.S. dollar as our functional currency. Foreign currency transaction gains and losses are included in income as they occur. The effect of foreign currency exchange rate fluctuations has not been significant to date. We do not use derivative financial instruments.

INVENTORY

Inventory is stated at the lower of cost or market, cost being determined under the first-in, first-out method.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 2--SIGNIFICANT ACCOUNTING POLICIES (CONTINUED)

PROPERTY AND EQUIPMENT

Property and equipment are stated at cost less accumulated depreciation. Depreciation is calculated on a straight-line basis over the asset's estimated useful life of two to seven years. Amortization of leasehold improvements is computed on a straight-line basis over the shorter of the facility lease term or the estimated useful lives of the improvements.

LONG-LIVED ASSETS

We review the impairment of long-lived assets whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. An impairment loss would be recognized when estimated future cash flows expected to result from the use of the asset and its eventual disposition is less than its carrying amount. No such impairment losses have been identified.

REVENUE RECOGNITION

Our FPGAs and ESPs may be programmed by the Company, the distributor or the end customer. We sell to certain distributors under agreements which, in the case of unprogrammed parts, allow certain rights of return and price adjustments on unsold inventory. Amounts billed to such distributors for shipments are included as accounts receivable, inventory is relieved, and the related revenue and cost of revenue are deferred and the resultant gross profit is recorded as a current liability, deferred income on shipments to distributors, until the inventory is resold by the distributor. Reserves for estimated returns and distributor price adjustments are provided against accounts receivable. Revenue for progammed parts, which do not have similar return rights, as well as for all non-distributor customers is recognized upon shipment. Software revenue is recognized when persuasive evidence of an agreement exists, delivery of the software has occurred, no significant Company obligations with regard to implementation or integration exist, the fee is fixed or determinable and collectibility is probable. Software revenues typically amount to less than 5% of total revenues.

STOCK-BASED COMPENSATION

We have elected to measure compensation costs using the intrinsic value method prescribed by APB Opinion No. 25, "Accounting for Stock Issued to Employees" and to comply with the pro forma disclosure requirements of Statement of Financial Accounting Standards No. 123, "Accounting for Stock-Based Compensation."

CONCENTRATION OF CREDIT RISK

Financial instruments which potentially subject us to concentrations of credit risk consist principally of cash and cash equivalents and accounts receivable. Cash and cash equivalents are maintained with high quality institutions. Our accounts receivable are derived primarily from sales to customers located in North America, Europe, Japan and Korea. We perform ongoing credit evaluations of our customers and generally do not require collateral. Bad debt write-offs to date have been immaterial.

At December 31, 1999, accounts receivable from two customers, both of which were distributors of our products, represent 21% and 16% of accounts receivable. At December 31, 1998, accounts receivable from the same two customers represented 15% and 18%, respectively, of accounts receivable.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 2--SIGNIFICANT ACCOUNTING POLICIES (CONTINUED)

LITIGATION LIABILITIES

We accrue for the cost of litigation in the period that costs become estimable and occurrence is determined to be probable. Accrued litigation liabilities of $6,500,000 at December 31, 1998 included estimated settlement costs and related legal fees (see Note 12).

SOFTWARE DEVELOPMENT COSTS

Software development costs incurred prior to the establishment of technological feasibility are included in research and development and are

expensed as incurred. Development costs incurred subsequent to the establishment of technological feasibility through the period of general market availability are capitalized, if material. To date, all software development costs have been expensed as incurred due to the insignificant development costs incurred during the short time period between the establishment of technological feasibility and general availability.

INCOME TAXES

We account for income taxes under the provisions of Statement of Financial Accounting Standards No. 109, "Accounting for Income Taxes" ("SFAS 109"). Under SFAS 109, deferred tax liabilities and assets are determined based on the differences between the financial statements and tax bases of assets and liabilities, using enacted tax rates in effect for the year in which the differences are expected to reverse.

OTHER COMPREHENSIVE INCOME (LOSS)

Effective January 1, 1998, we adopted the provisions of Statement of Financial Accounting Standards No. 130, "Reporting Comprehensive Income" ("SFAS 130"). SFAS 130 establishes standards for reporting comprehensive income (loss) and its components in financial statements. Comprehensive income (loss) as defined, includes all changes in equity (net assets) during a period from nonowner sources. No items were included in other comprehensive income (loss) during 1997, 1998 and 1999.

NEW ACCOUNTING PRONOUNCEMENTS

In December 1999, the Securities and Exchange Commission (SEC) issued Staff Accounting Bulletin No. 101 (SAB101), "Revenue Recognition in Financial Statements." SAB101 summarizes certain of the SEC's views in applying generally accepted accounting principles (GAAP) to revenue recognition in financial statements. We are required to adopt SAB101 in the first quarter of fiscal 2000 and are currently studying the impact of SAB 101 on our financial statements. We do not believe that SAB101 will have a material impact on our financial statements.

In June 1998, the FASB issued SFAS No. 133, "Accounting for Derivative Instruments and Hedging Activities." SFAS No. 133 established a model for accounting for derivatives and hedging activities and supercedes and amends a number of existing accounting standards. SFAS No. 133 requires that all derivatives be recognized in the balance sheet at their fair market value, and the corresponding derivative gains or losses be either reported in the statement of operations or as a deferred item depending on the type of hedge relationship that exists with respect to such derivative. SFAS No. 133, as amended by SFAS No. 137, "Accounting for Derivative Instruments and Hedging Activities--Deferral of Effective Date of FASB Statement No. 133," is effective for all fiscal quarters and years beginning after June 15, 2000. We do

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 2--SIGNIFICANT ACCOUNTING POLICIES (CONTINUED)
not currently, nor do we plan to, enter into forward exchange contracts to hedge exposures denominated in foreign currencies or any other derivative financial instruments for trading or speculative purposes.

NOTE 3--NET INCOME (LOSS) PER SHARE

Basic earnings per share (EPS) is computed by dividing net income available to common stockholders (numerator) by the weighted average number of common shares outstanding (denominator) during the period. Diluted EPS is computed using the weighted average number of common shares and dilutive potential common shares outstanding during the period. In computing diluted EPS, the average stock price for the period is used in determining the number of share assumed to be purchased from the exercise of stock options. A reconciliation of the numerators and denominators of the basic and diluted per share computations is as follows (in thousands, except per share amounts):

<TABLE>
<CAPTION>

	DECEMBER 31,		
	1997	1998	1999

<S>	<C>	<C>	<C>
Numerator:			
Net income (loss)	$(33,648)	$ 245	$ 3,161
Denominator:			
Common stock	1,005	3,490	7,618
Common stock to be issued	2,278	759	--
Less: Unvested common stock option exercises	(51)	(18)	(3)
Weighted average shares outstanding for basic	3,232	4,231	7,615
Convertible preferred stock	--	9,912	7,434
Stock options and warrants	--	484	1,348
Unvested common stock option exercises	--	18	3
Weighted average shares outstanding for diluted	$ 3,232	$14,645	$16,400
Net income (loss) per share			
Basic	$ (10.41)	$ 0.06	$ 0.42
Diluted	$ (10.41)	$ 0.02	$ 0.19

As a result of the net losses incurred by us during fiscal year 1997, all potential common shares, amounting to 11,991,000 shares, were anti-dilutive and have been excluded from the diluted net loss per share calculation. For fiscal years 1998 and 1999, all potential common shares have been included in the calculation of diluted EPS.

NOTE 4--BALANCE SHEET COMPONENTS

	DECEMBER 31,	
	1998	1999
	(IN THOUSANDS)	
<S>	<C>	<C>
Inventory:		
Raw materials	$ 56	$ 183
Work-in-process	2,611	3,642
Finished goods	210	524
	$ 2,877	$ 4,349
Property and equipment:		
Equipment	$ 4,733	$ 6,271
Software	1,059	1,795
Furniture and fixtures	761	757
Leasehold improvements	564	563
	7,117	9,386
Accumulated depreciation	(4,225)	(4,876)
	$ 2,892	$ 4,510
Accrued liabilities:		
Accrued employee compensation	$ 935	$ 1,356
Other liabilities	1,490	1,049
	$ 2,425	$ 2,405

NOTE 5--LONG-TERM OBLIGATIONS

	DECEMBER 31,	
	1998	1999
	(IN THOUSANDS)	
Installment notes payable to bank	$ 966	$ 561
Installment notes payable to vendor	--	--
Litigation accrual	6,500	--
Other	311	283
	7,777	844
Current portion of long-term obligations	(7,186)	(716)
Long-term obligations	$ 591	$ 128

At December 31, 1998 and 1999, we had outstanding bank installment notes totaling $966,000 and $561,000, respectively. The notes bear interest at prime plus 0.25% (8.75% as of December 31, 1999), and are secured by the specific equipment financed. Principal payments are due in equal monthly installments over the term of the notes which mature in 2000 and 2002. At December 31, 1998, we were in violation of the bank covenants. Subsequently, we obtained a waiver for the covenants. In the quarter ended June 30, 1999 we entered into an extension to borrow up to $250,000 using bank installment notes which are

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 5--LONG-TERM OBLIGATIONS (CONTINUED)
secured by the specific equipment financed. At December 31, 1999, we had borrowed $250,000 under this facility. These notes mature in 2002. At December 31, 1999, we were in compliance with its covenants.

In August 1998, we settled our lawsuit with Actel Corporation. The obligation for settlement and legal cost was payable quarterly through August 2001, subject to acceleration upon the completion of our initial public offering. We paid our remaining obligation of $5.75 million on November 3, 1999. (see Note 12).

NOTE 6--INCOME TAXES

No provision for federal or state income taxes has been recorded for the year ended December 31, 1997 as the Company incurred an operating loss. No provision for federal or state income taxes has been recorded for the years ended December 31, 1998 and 1999 as the Company had the ability to utilize federal and state net operating loss carryforwards.

A rate reconciliation between income tax provisions at the US federal statutory rate and the effective rate reflected in the Consolidated Statement of Operations is as follows:

	YEAR ENDED DECEMBER 31,		
	1997	1998	1999
Provision at statutory rate	(34)%	34	34
Utilization of operating loss and credit carryforwards	--	(34)	(34)
Future benefit of deferred tax assets not recognized	34	--	--
	--%	--%	--%

The Company did not have any significant foreign tax liability during the periods presented.

Deferred tax balances are comprised of the following:

<TABLE>
<CAPTION>

	DECEMBER 31,	
	1998	1999
<S>	<C>	<C>
Deferred tax assets:		
Net operating loss carryforward	$ 15,728	$ 15,396
Accruals and reserves	5,970	4,725
Credit carryforward	2,351	3,245
Capitalized research and development	633	559
	24,682	23,925
Valuation allowances	(24,682)	(23,925)
Deferred tax asset	$ --	$ --

</TABLE>

Management believes that, based on a number of factors, the available objective evidence creates sufficient uncertainty regarding the realizability of the deferred tax assets such that a full valuation allowance has been recorded. These factors include the Company's history of losses, that the market in which the Company competes is intensely competitive and characterized by rapidly changing technology, the lack of carryback capacity to realize deferred tax assets, and uncertainty regarding market acceptance of the Company's products. The Company will continue to assess the realizability of the deferred tax assets in future periods.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 6--INCOME TAXES (CONTINUED)

At December 31, 1999, the Company had net operating loss carryforwards for federal and state income tax purposes of approximately $42 million and $21 million, respectively. These carryforwards, if not utilized to offset future taxable income and income taxes payable, will expire in the years 2000 through 2017.

Under the Tax Reform Act of 1986, the amount of and the benefit from net operating losses that can be carried forward may be impaired in certain circumstances. Events which may cause changes in the Company's tax carryovers include, but are not limited to, a cumulative ownership change of more than 50% over the three year period. Since inception, the Company believes cumulative changes in ownership have invoked the loss carryforward deduction limitation under IRC Section382. However, the Company believes that such limitations will not have a material effect on the future utilization of the losses.

NOTE 7--STOCKHOLDERS' EQUITY

CONVERTIBLE PREFERRED STOCK

At December 31, 1998, the Company had 9,912,000 shares of Series A, B, C, D, E and F preferred stock outstanding. The holders of the outstanding Series A, B, C, D, E and F preferred stock were entitled to certain dividend and liquidation preference rights. No dividends were declared or paid related to preferred stock. Each share of preferred stock was convertible at the option of the holder, or upon the Company's completion of a qualifying public offering of common stock. Upon completion of the Company's initial public offering on October 15, 1999, each share of Series A, B, C, D, E and F preferred stock was converted into one share of the Company's common stock.

COMMON STOCK

In March 1997, in conjunction with the issuance of series F preferred stock, the Company authorized an additional 20,000,000 shares of common stock for a

total authorized amount of 105,000,000 shares.

The Company was originally incorporated in California in April 1988. In October 1999 the Company reincorporated in Delaware and, in conjunction with that reincorporation, effected a 1-for-6 stock split (the "Reverse Stock Split") of its preferred stock and common stock. All references to the number of shares of preferred stock, common stock and per share amounts have been retroactively restated in the accompanying financial statements to reflect the effect of the Reverse Stock Split. The Board of Directors also approved a recapitalization that authorized 100 million shares of common stock and ten million shares of undesignated preferred stock.

The Company completed an initial public offering of its common stock on October 15, 1999. The underwriters' over-allotment option was exercised and QuickLogic sold a total of 3,770,635 common shares at $10.00. Proceeds, net of underwriting discounts and commissions and related offering expenses, of $33.9 million were received.

EMPLOYEE STOCK OPTION PLANS

1989 STOCK OPTION PLAN

In July 1996, the 1989 Stock Plan (the "1989 Plan") was amended to allow options to be exercised prior to vesting. Unvested shares are deposited to an escrow agent and the Company has a right to repurchase unvested shares at the original issuance price if the employee is terminated. In April 1999, an

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 7--STOCKHOLDERS' EQUITY (CONTINUED)
additional 1,333,000 shares were authorized for issuance. The 1989 Plan provides for the issuance of incentive and nonqualified options for the purchase of up to 4,617,000 shares of Common Stock. Options may be granted to employees, directors and consultants to the Company. The fair value of the Company's common stock was determined by the Board of Directors considering operating results, current legal developments, product life cycle, general market conditions, independent valuations and other relevant factors. Options granted under the 1989 Plan may have a term of up to 10 years. Options typically vest at a rate of 25% of the total grant per year over a four-year period. However, the Company may, at its discretion implement a different vesting schedule with respect to any new stock option grant. In September 1999, the Company adopted the 1999 Stock Option Plan and all subsequent stock option grants are made under this later plan.

1999 STOCK OPTION PLAN

The 1999 Stock Plan (the "1999 Plan") was adopted by the Board of Directors in August 1999 and was approved by the stockholders in September 1999. The total number of shares of common stock reserved for issuance under this plan is 5,000,000 shares of common stock. In addition, commencing January 2000, an annual increase will be added to the 1999 stock plan equal to the lesser of 5,000,000 shares or 5% of the outstanding shares on such date. Options granted under the 1999 Plan may have a term of up to 10 years. Options typically vest at a rate of 25% of total grants per year over a four-year period. However, the Company may, at its discretion implement a different vesting schedule with respect to any new stock option grant.

The following table summarizes all of our stock option activity under the 1989 Plan and the 1999 Plan and related weighted average exercise price for the years ended December 31, 1997, 1998 and 1999:

<TABLE>
<CAPTION>

	OPTIONS OUTSTANDING	WEIGHTED AVERAGE EXERCISE PRICE
	(IN THOUSANDS)	
<S>	<C>	<C>
Balance at December 31, 1996	1,284	$0.66
Granted	1,636	4.53
Canceled	(558)	5.30
Exercised	(356)	0.88

Balance at December 31, 1997	2,006	2.49
Granted	1,151	4.50
Canceled	(703)	3.26
Exercised	(89)	1.30
Balance at December 31, 1998	2,365	3.26
Granted	1,624	8.60
Canceled	(482)	5.10
Exercised	(142)	3.06
Balance at December 31, 1999	3,365	$5.64

</TABLE>

As of December 31, 1999, 5,345,000 shares were available for grant, 3,000 unvested shares had been exercised and remain subject to our buyback rights and options to purchase 2,834,000 shares were vested.

NOTE 7--STOCKHOLDERS' EQUITY (CONTINUED)

At December 31, 1998 and 1997, options to purchase 1,601,000 and 1,936,000 shares, respectively, were vested.

On October 20, 1997, we repriced options to purchase 316,000 shares of common stock that were issued to employees at exercise prices of $6.00 to $9.00 between April and September 1997 to an exercise price of $4.50. The original vesting terms of these options remained unchanged.

Related weighted average exercise price and contractual life information at December 31, 1999 are as follows:

<TABLE>
<CAPTION>

	OPTIONS			OPTIONS	
	OPTIONS	WEIGHTED AVERAGE		VESTED AND	
RANGE OF	OUTSTANDING AS OF	REMAINING	WEIGHTED AVERAGE	EXERCISABLE AS OF	WEIGHTED AVERAGE
EXERCISE PRICES	DECEMBER 31, 1999	CONTRACTUAL LIFE	EXERCISE PRICE	DECEMBER 31, 1999	EXERCISE PRICE
	(IN THOUSANDS)	(IN YEARS)			
<S>	<C>	<C>	<C>	<C>	<C>
$0.30-$0.60	448	4.8	$ 0.59	448	$0.59
2.40-4.50	1,490	8.0	3.97	1,490	3.97
4.86-6.00	472	9.3	5.53	472	5.53
$6.78-$15.24	955	9.8	10.59	424	6.78
	3,365	8.3		2,834	

</TABLE>

The weighted average estimated grant date fair values, as defined by SFAS 123, for options granted during 1997, 1998 and 1999 was $2.52, $1.02 and $3.80 per option, respectively. The fair value of each option grant is estimated on the date of grant using the Black-Scholes option pricing model. The Black-Scholes model, as well as other currently accepted option valuation models, was developed to estimate the fair value of freely tradable, fully transferable options without vesting restrictions, which significantly differ from our stock option awards.

The following weighted average assumptions are included in the estimated grant date fair value calculations for stock option grants in 1997, 1998 and 1999:

<TABLE>
<CAPTION>

	DECEMBER 31,		
	1997	1998	1999
<S>	<C>	<C>	<C>
Expected life (years)	5.3	5.3	5.3
Risk-free interest rate	6.20%	4.99%	4.99%

Volatility	--	--	65%
Dividend yield	--	--	--

EMPLOYEE STOCK PURCHASE PLAN

The 1999 Employee Stock Purchase Plan ("ESPP") was also adopted by the Board of Directors in August 1999 and was approved by the stockholders in September 1999. The total number of shares of common stock reserved for issuance under this plan is 2,000,000 plus annual increases equal to the lesser of 1,500,000 shares or 4% of the outstanding shares on such date. The ESPP contains consecutive, overlapping, twenty-four month offering periods. Each offering period includes four six-month purchase periods. The ESPP permits participants to purchase shares through payroll deductions of up to 20% of an employee's total compensation (maximum of 20,000 shares) at 85% of the lower of the fair market value of the common stock at the beginning or end of a purchase period.

NOTE 7--STOCKHOLDERS' EQUITY (CONTINUED)

The following weighted average assumptions are included in the estimated grant date fair value calculations for rights to purchase stock under ESPP:

	DECEMBER 31,
	1999
Expected life	6 months
Risk-free interest rate	5.00%
Volatility	65%
Dividend yield	--

The weighted average estimated grant date fair value of rights to purchase common stock under the ESPP was $4.03.

Had the Company recorded compensation cost based on the estimated grant date fair value, as defined by SFAS 123, for awards granted under its stock option and employee stock purchase plans, its pro forma net loss would have been as follows for the years ended December 31, 1997, 1998 and 1999:

	DECEMBER 31,		
	1997	1998	1999
	(IN THOUSANDS, EXCEPT PER SHARE AMOUNTS)		
Pro forma net income (loss)	$(33,953)	$ (663)	$1,650
Pro forma net income (loss) per share:			
Basic	$ (10.51)	$(0.16)	$ 0.22
Diluted	$ (10.51)	$(0.16)	$ 0.11

DEFERRED COMPENSATION

During the year ended December 31, 1997, 1998, 1999 the Company granted options to purchase 833,000, 139,000 and 866,000 shares of common stock, respectively, at a price less than the fair market value of its common stock at the time of the grant and recorded related deferred compensation of $1,890,000, $204,000 and $908,000, respectively, net of reversals associated with unvested shares of terminated employees. Such deferred compensation is being amortized ratably over the vesting period of the options.

NOTE 8--RELATED PARTY TRANSACTIONS

In October 1992, in conjunction with the issuance of Series D preferred stock, the Company entered into a Technical Transfer, Joint Development License

and Foundry Supply Agreement (the "Existing Agreement") with Cypress Semiconductor Corporation ("Cypress"). Cypress owns 100% of the Company's Series D preferred stock. The agreement provides that the Company and Cypress share processing technologies and licenses to market developed FPGA products and that Cypress guarantees the Company certain wafer start capacity. The Company purchased all of its wafers under this agreement during 1997.

In March 1997, the Company and Cypress terminated the Existing Agreement, and replaced it with a new arrangement whereby the Company's FPGA products will no longer be second sourced by Cypress. In exchange for the termination of the Existing Agreement and the reversion of the rights to the intellectual property developed thereunder to the Company, the Company paid $4.5 million in cash and agreed to

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 8--RELATED PARTY TRANSACTIONS (CONTINUED)
issue 3,037,786 shares of Common Stock to Cypress, resulting in a charge of approximately $23.0 million in the first quarter of 1997. The Company's revenue and net income were not measurably enhanced by the termination of the Existing Agreement nor the reversion of the related rights to the Company-developed intellectual property. The 3,037,786 shares of Common Stock were issued to Cypress on April 1, 1998. In addition, the Company granted Cypress certain contractual rights as to the shares of the Company's stock held by Cypress, including the right to sell shares in an initial public offering. The parties also entered into a new foundry agreement and a cross-license agreement.

NOTES RECEIVABLE FROM STOCKHOLDER

As of December 31, 1998 and 1999, we had $121,000 of demand promissory notes due from a stockholder. The notes bear interest at rates ranging from 6.7% to 8.5% per annum and are secured by shares of our common stock held by the stockholder.

NOTE 9--MANUFACTURING AGREEMENT

In July 1997, the Company entered into a manufacturing agreement with Taiwan Semiconductor Manufacturing Company, Ltd. ("TSMC") for a term of three years renewable annually as a rolling three-year agreement. The agreement guarantees certain capacity availability and requires that a minimum percentage of the total number of wafers required by the Company in any one year are purchased from TSMC (excluding wafers purchased from Cypress and certain other wafer requirements), and requires "take or pay" volume commitments twelve months in length based upon usage forecasts supplied by the Company. Obligations are payable in U.S. dollars. However, the purchase price for wafers shall be adjusted for any fluctuation in the New Taiwan Dollar exchange rate greater than 5%. The Company has committed to purchase approximately $9.4 million under this agreement in 2000. Purchases under this agreement totaled $202,000, $1.0 million and $2.1 million in 1997, 1998 and 1999, respectively.

NOTE 10--INFORMATION CONCERNING BUSINESS SEGMENTS AND MAJOR CUSTOMERS

INFORMATION ABOUT GEOGRAPHIC AREAS

All of our sales originate in the United States. Shipments to some of our distributors are made to centralized purchasing and distributing locations, which in turn sell through to other locations. As a result of these factors, we believe that sales to certain geographic locations might be higher or lower, though accurate data is difficult to obtain.

The following is a breakdown of revenues by shipment destination for the years ended 1997, 1998 and 1999:

<TABLE>
<CAPTION>

	DECEMBER 31,		
	1997	1998	1999
	(IN THOUSANDS)		
<S>	<C>	<C>	<C>
United States	$16,222	$15,784	$20,681
Japan	3,357	3,162	5,033

Europe	3,886	4,752	4,871
Rest of world	4,995	6,309	9,200
	$28,460	$30,007	$39,785

</TABLE>

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 10--INFORMATION CONCERNING BUSINESS SEGMENTS AND MAJOR CUSTOMERS (CONTINUED)

The countries comprising "Rest of world" category include Canada, the UK, Korea and other countries in Asia, none of which individually comprise more than 10% of our sales.

Three customers, distributors of our products, accounted for approximately 24%, 11% and 10% of revenues in 1999. Three customers, distributors of our products, accounted for approximately 27%, 10% and 10% of revenues in 1998. Three customers, distributors of our products, accounted for approximately 20%, 15% and 13% of revenue in 1997. All sales are made from the United States and are denominated in U.S. dollars.

Less than 10% of our long-lived assets, including property and equipment and other assets, were located outside the United States.

NOTE 11--COMMITMENTS

We lease our primary facility under a noncancelable operating lease which expires in 2003, and includes an option to renew through 2006. The lease is secured by a $300,000 certificate of deposit that matures in 2000. Rent expense for the years ended December 31, 1997, 1998 and 1999 was approximately $478,000, $531,000, and $628,000 respectively.

We also lease certain equipment and leasehold improvements under capital leases, which expire in 2003. Assets acquired under capital leases and included in plant and equipment at December 31, 1997, 1998, and 1999, were $232,000, $232,000 and $198,000 respectively.

Future minimum lease commitments, excluding property taxes and insurance, are as follows:

<TABLE>
<CAPTION>

	OPERATING LEASES	CAPITAL LEASES
	(IN THOUSANDS)	
<S>	<C>	<C>
Year Ending December 31,		
2000	$ 584	$ 67
2001	680	67
2002	710	67
2003	630	46
2004 and thereafter	50	--
	$2,654	247
Less amount representing interest		(49)
Present value of capital lease obligations		198
Less current portions		(70)
Long-term portion of capital lease obligations		$128

</TABLE>

NOTE 12--LITIGATION

In September 1999, we received an offer to license a patent related to field programmable gate array architecture. It is too early for us to determine whether this license would be necessary or useful, or whether a license would be obtainable at a reasonable price. Offers such as this may lead to litigation if we

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS (CONTINUED)

NOTE 12--LITIGATION (CONTINUED)
reject the opportunity to obtain the license. We believe that the resolution of this matter will not have a material adverse effect on our financial condition or results of operations.

The semiconductor industry has experienced a substantial amount of litigation regarding patent and other intellectual property rights. From time to time, we have received and may receive in the future, communications alleging that our products or our processes may infringe on product or process technology rights held by others. We may in the future be involved in litigation with respect to alleged infringement by us of another party's patents. In the future, we may be involved with litigation to:

- Enforce our patents or other intellectual property rights.

- Protect our trade secrets and know-how.

- Determine the validity or scope of the proprietary rights of others.

- Defend against claims of infringement or invalidity.

- Such litigation has in the past and could in the future result in substantial costs and diversion of management resources. Such litigation could also result in payment of substantial damages and/or royalties or prohibitions against utilization of essential technologies, and could have a material adverse effect on our business, financial condition and results of operations.

LITIGATION SETTLEMENT

During 1994, Actel Corporation ("Actel"), a competitor of the Company, filed a lawsuit seeking unspecified damages and alleging that our products infringe upon its patents. We countersued alleging that Actel's products infringed on our patents. During 1995 and 1996, Actel's suit was amended to include a trade misappropriation claim and additional patent infringement claims. Actel and the Company settled their litigation in August 1998. The Company and Actel have granted each other non-exclusive, royalty free, worldwide, perpetual cross licenses of their existing technology, excluding only certain SRAM technology owned by Actel. We have made quarterly payments to Actel since the settlement date. The remainder of the settlement was paid to Actel immediately after our initial public offering. We paid all of our remaining obligation under the settlement on November 3, 1999.

NOTE 13--SUBSEQUENT EVENT (UNAUDITED)

On March 20, 2000, we filed a registration statement with the Securities and Exchange Commission for a proposed offering of 4,568,059 shares of our common stock. Of the shares included in the offering, it is expected that approximately 1,500,000 shares will be offered by us, and 3,068,059 shares will be offered for resale by selling stockholders.

ITEM 9. CHANGES IN AND DISAGREEMENTS WITH ACCOUNTANTS ON ACCOUNTING AND FINANCIAL DISCLOSURE.

Not applicable.

PART III

Certain information required by Part III is omitted from this Report in that the registrant will file a definitive Proxy Statement pursuant to Regulation 14A (the "Proxy Statement") not later than 120 days after the end of the fiscal year covered by this Report, and certain information therein is incorporated herein by reference.

ITEM 10. DIRECTORS AND OFFICERS OF THE COMPANY

Certain information regarding the directors and officers of the Company is contained herein under Item 1, "Executive Officers and Directors of the Company."

Information regarding directors appearing under the caption "Election of Directors--Directors and Nominees for Director" in the Proxy Statement is hereby incorporated by reference.

Information regarding compliance with Section 16(a) of the Securities Exchange Act of 1934, as amended, is hereby incorporated herein by reference from the section entitled "Election of Directors--Section 16(a) Beneficial Ownership Reporting Compliance" in the Proxy Statement.

ITEM 11. EXECUTIVE COMPENSATION

The information required by Item 11 is set forth under the caption, "Executive Compensation" in our Proxy Statement, which information is incorporated herein by reference.

ITEM 12. SECURITY OWNERSHIP OF CERTAIN BENEFICIAL OWNERS AND MANAGEMENT

The information required by Item 12 is set forth under the caption "Security Ownership" in our Proxy Statement, which information is incorporated herein by reference.

ITEM 13. CERTAIN RELATIONSHIPS AND RELATED TRANSACTIONS

The information required by Item 13 is set forth under the captions "Compensation Committee Interlocks and Insider Participation" and "Related Party Transactions" in our Proxy Statement, which information is incorporated herein by reference.

PART IV

ITEM 14. EXHIBITS, FINANCIAL STATEMENT SCHEDULE AND REPORTS ON FORM 8-K

(a) 1. Financial Statement

Reference is made to page 36 for a list of all financial statements and scheduled filed as a part of this report.

2. Financial Statement Schedules

QUICKLOGIC CORPORATION
VALUATION AND QUALIFYING ACCOUNTS
(IN THOUSANDS)

<TABLE>
<CAPTION>

DESCRIPTION	BALANCE AT BEGINNING OF PERIOD	CHARGED TO COSTS AND EXPENSES	CHARGED TO OTHER ACCOUNTS	DEDUCTIONS	BALANCE AT END OF PERIOD
<S>	<C>	<C>	<C>	<C>	
Allowance for Doubtful Accounts					
Year ended December 31, 1999.....	$ 245	--	--	(51)	$ 194
Year ended December 31, 1998.....	$ 226	29	--	(10)	$ 245
Year ended December 31, 1997.....	$ 105	121	--	--	$ 226
Sales Returns and Allowance Reserve					
Year ended December 31, 1999.....	$3,027	7,099	--	(9,015)	$1,111
Year ended December 31, 1998.....	$2,402	5,002	--	(4,377)	$3,027
Year ended December 31, 1997.....	$1,979	5,880	--	(5,457)	$2,402

</TABLE>

All other schedules not listed above have been omitted because the information required to be set forth therein is not applicable or is shown in the financial statements or notes hereto.

3. Exhibits

The exhibits listed under Item 14(c) hereof are filed as part of this Annual Report on Form 10-K.

(b) Reports on Form 8-K.

No reports on Form 8-K were filed during the last quarter of the period covered by this report.

(c) Exhibits

The following exhibits are filed with this report:

EXHIBIT NUMBER	DESCRIPTION
3.1(1)	Amended and Restated Certificate of Incorporation of the Registrant.
3.2(1)	Bylaws of the Registrant.
4.1(1)	Specimen Common Stock certificate of the Registrant.
10.1(1)	Form of Indemnification Agreement for directors and executive officers.
10.2(1)	1999 Stock Plan and form of Option Agreement thereunder.
10.3(1)	1999 Employee Stock Purchase Plan.
10.4(1)	1989 Stock Option Plan.

EXHIBIT NUMBER	DESCRIPTION
10.5(1)	Series F Preferred Stock Purchase Agreement dated November 27, 1996 and January 24, 1997 by and among the Registrant and the Purchasers named therein.
10.6(1)	Termination Agreement dated March 29, 1997 between the Registrant and Cypress Semiconductor Corporation.
10.7(1)	Cross License Agreement dated March 29, 1997 between the Registrant and Cypress Semiconductor Corporation.
10.8(1)	Wafer Fabrication Agreement March 29, 1997 between the Registrant and Cypress Semiconductor Corporation.
10.9(1)	Sixth Amended and Restated Shareholder Agreement dated March 29, 1997 by and among the Registrant, Cypress Semiconductor Corporation and certain stockholders.
10.10(1)	Sixth Amended and Restated Registration Rights Agreement dated March 29, 1997 by and among the Registrant, Cypress and certain stockholders.
10.11(1)	Technical Transfer, Joint Development License and Foundry Supply Agreement, dated October 2, 1992, between the Registrant and Cypress.
10.12(1)	Lease dated June 17, 1995, as amended, between Kairos, LLC and Moffet Orchard Investors as Landlord and the Registrant for the Registrant's facility located in Sunnyvale, California.
10.13(1)	Business Loan Agreement dated August 9, 1995 between the Registrant and Silicon Valley Bank, as amended.
10.14(1)	Loan and Security Agreement dated August 8, 1996 between the Registrant and Silicon Valley Bank, as amended.
10.15(1)	Export-import Bank Loan and Security Agreement dated August 8, 1996 between the Registrant and Silicon Valley Bank.
10.16(1)	First Amended and Restated Common Stock Purchase Agreement

dated June 13, 1997 between the Registrant and Cypress.

10.17(1) Take or Pay Agreement dated July 21, 1997 between the Registrant and Taiwan Semiconductor Manufacturing Company, Ltd.

10.18(1) Patent Cross License Agreement, dated August 25, 1998, between the Registrant and Actel Corporation.

16.1(1) Letter of Deloitte & Touche LLP, Independent Accountants, dated July 28, 1997 regarding change in certifying accountant.

21.1(1) Subsidiary of the Registrant.

24.1 Power of Attorney-See page II-5.

27.1 Financial Data Schedule.
</TABLE>

- ----------

(1) Incorporated by reference to Registrant's Registration Statement on Form S-1 declared effective October 14, 2000 (Commission File No. 333-28833).

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Act of 1933, as amended, the Registrant has duly caused report to be signed on its behalf by the undersigned, thereunto duly authorized on this 30th day of March, 2000.

<TABLE>
<S> <C> <C>
QUICKLOGIC CORPORATION, INC.

By: /s/ E. THOMAS HART

E. Thomas Hart
PRESIDENT AND CHIEF EXECUTIVE OFFICER
</TABLE>

POWER OF ATTORNEY

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints E. Thomas Hart and Arthur O. Whipple and each of them singly, as true and lawful attorneys-in-fact and agents with full power of substitution and resubstitution, for him and in his name, place and stead, in any and all capacities to sign this Annual Report on Form 10-K filed herewith and any or all amendments to said report, and to file the same, with all exhibits thereto, and other documents in connection therewith, with the Securities and Exchange Commission granting unto said attorneys-in-fact and agents the full power and authority to do and perform each and every act and the thing requisite and necessary to be done in and about the foregoing, as to all intents and purposes as he or she might or could do in person, hereby ratifying and confirming all that said attorneys-in-fact and agents or any of them, or his substitute, may lawfully do or cause to de done by virtue hereof.

Pursuant to the requirements of the Securities Act of 1933, as amended, this report has been signed by the following persons in the capacities and on the dates indicated below.

<TABLE>
<CAPTION>
SIGNATURE	CAPACITY IN WHICH SIGNED	DATE
<C>	<S>	<C>
/s/ E. THOMAS HART E. Thomas Hart	President, Chief Executive Officer and Director (Principal Executive Officer)	March 30, 2000
/s/ ARTHUR O. WHIPPLE	Vice President, Finance, Chief Financial Officer and	
</TABLE>

---------- Arthur O. Whipple	Secretary (Principal Financial Officer)	March 30, 2000
/s/ IRWIN B. FEDERMAN ---------- Irwin B. Federman	Director	March 30, 2000
/s/ HUA-THYE CHUA ---------- Hua-Thye Chua	Director	March 30, 2000
/s/ DONALD P. BEADLE ---------- Donald P. Beadle	Director	March 30, 2000
---------- Michael J. Callahan	Director	March 30, 2000

</TABLE>

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<SALES> 39,785
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<CGS> 17,103
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